

Next-Gen GaN Power Electronics: Overcoming the Multi-MHz Challenge

Miroslav Vasić - miroslav.vasic@upm.es

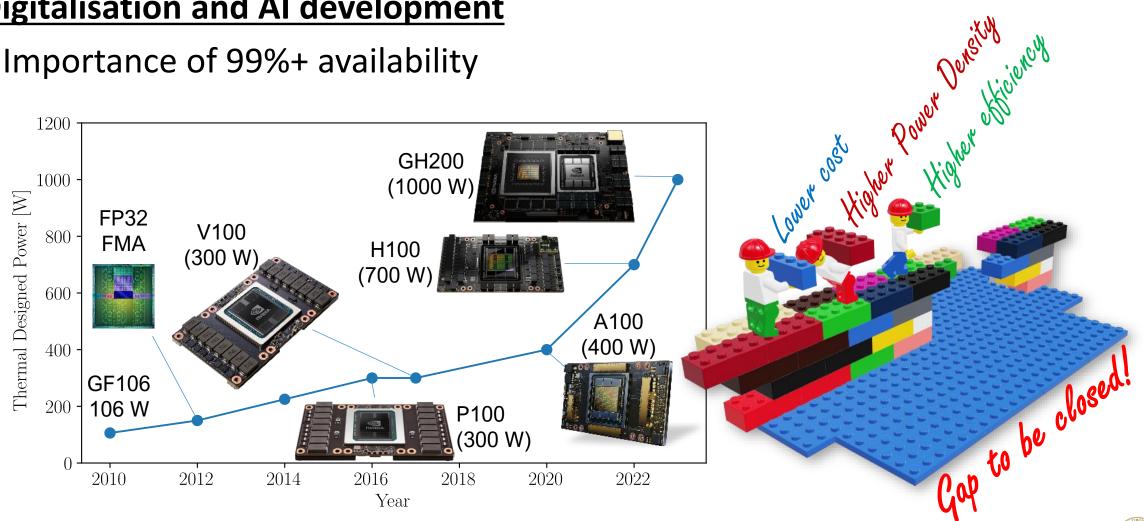




Introduction – Global Megatrends

Digitalisation and AI development

Importance of 99%+ availability



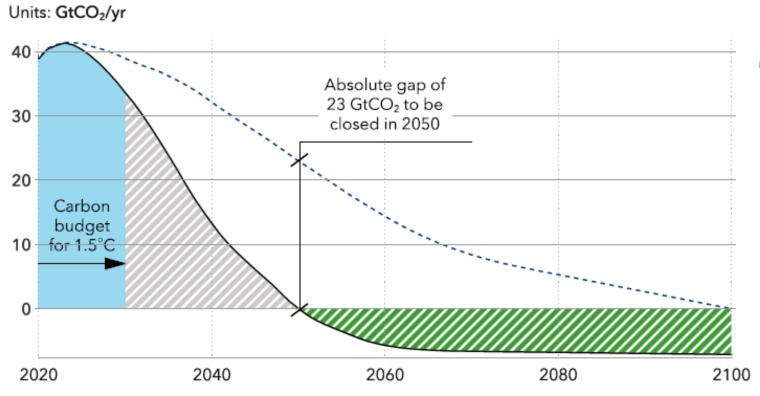


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Introduction – Global Megatrends

Carbon dioxide emissions

Cut by 19% by 2030



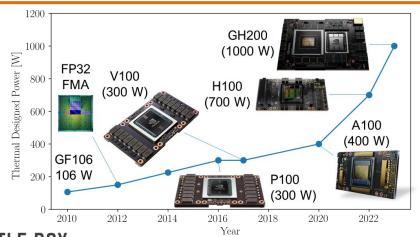
 The CO₂ emissions are expected to reach record levels in 2023

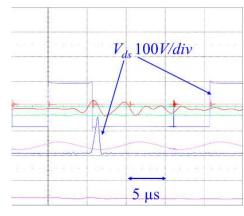
Immediate reaction is needed!



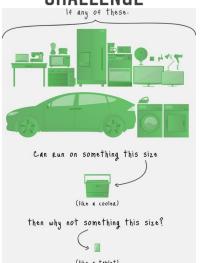


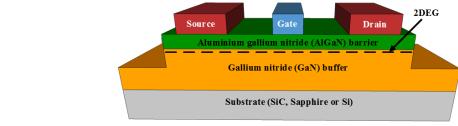
GaN HEMT – What's your first thought?

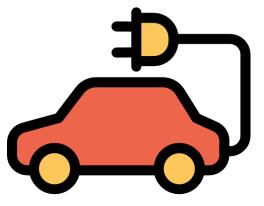


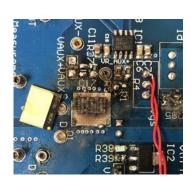


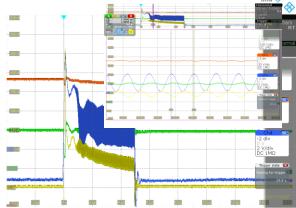












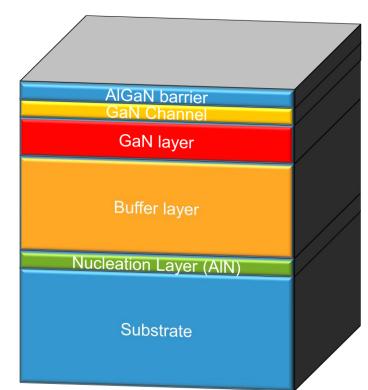


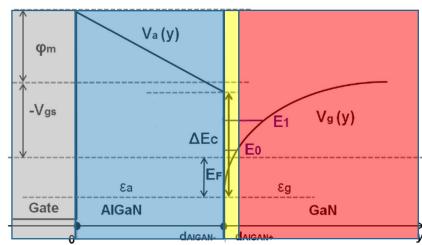


HEMT Structure – enables low Coss

- Simplified visualization
- No pn junction → lower capacitance

- Device isolation and improves the material quality
- Base to build GaN transistor
- To ensure better growth quality of the following layers
- Lattice transition from Si to GaN
- Silicon
- Wafer thickness (300 μm 500 μm)



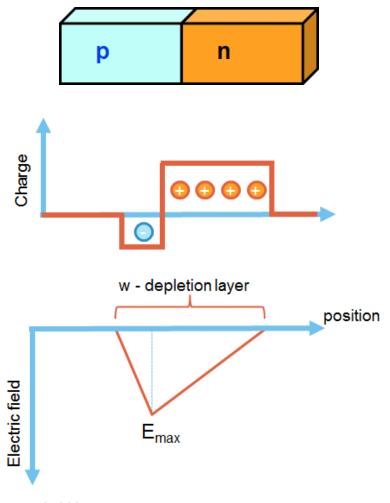


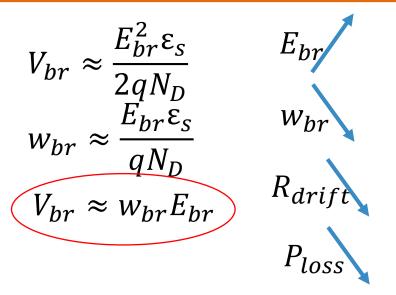




pn junction - break down voltage

Correlation between E_c and R_{on}





Just to refresh your memory...

$$E_{critical}$$

 $Si = 0.3x10^6 \, V/cm$
 $GaN, SiC \, 3x10^6 \, V/cm$

This is the main reason for the SiC and GaN superiority!





Semiconductor technology limit – 1D approximation

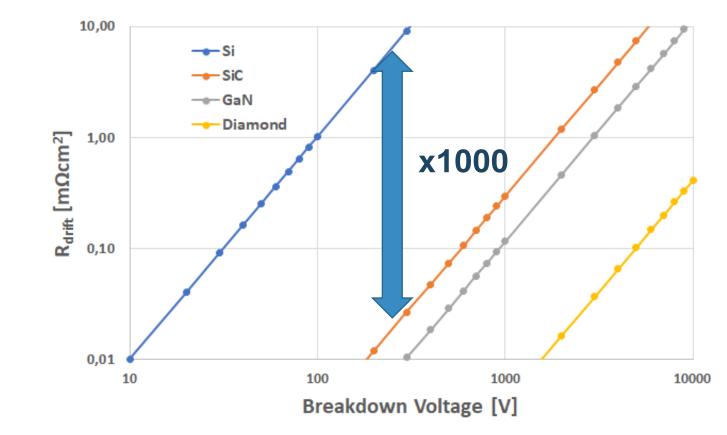
- Baliga Figure of Merit
- Not the best approximation

We start with:

$$V_{br} \approx \frac{E_{br}^2 \varepsilon_s}{2qN} \quad w_{br} \approx \frac{E_{br} \varepsilon_s}{qN}$$

$$R_{drift} = \frac{w_D}{qN_D\mu_D}$$

$$R_{drift} = \frac{4V_{br}^2}{\mu_D E_{br}^3 \varepsilon_s}$$

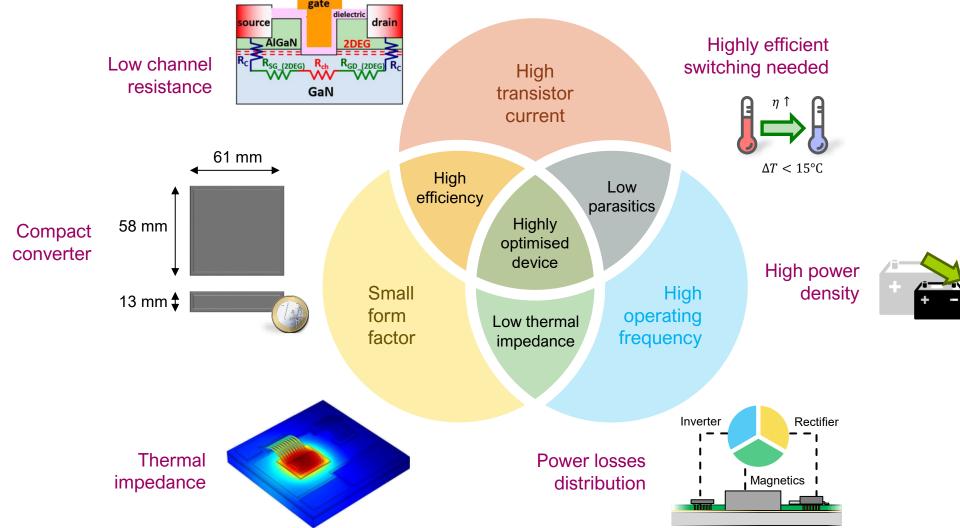


- Direct consequence of E_{br}!
- Very optimistic prediction!





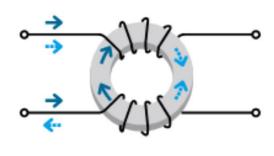
Motivation – High Performance



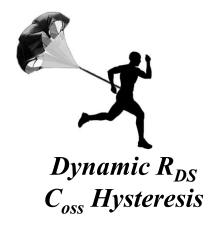


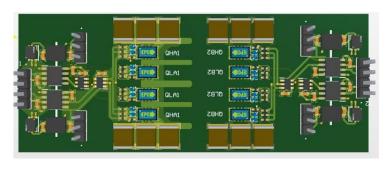


What we will see in this talk?

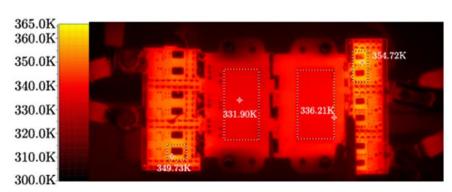


CM Currents



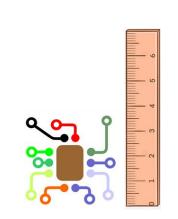


Layout optimization



Thermal behaviour







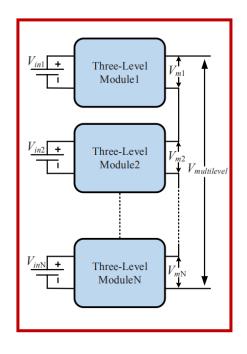
Short Circuit Capability

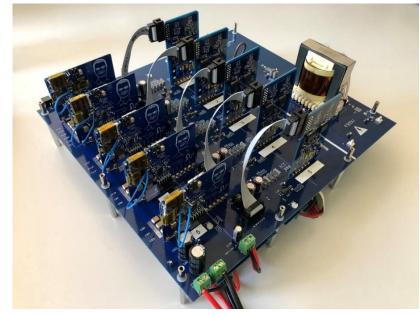




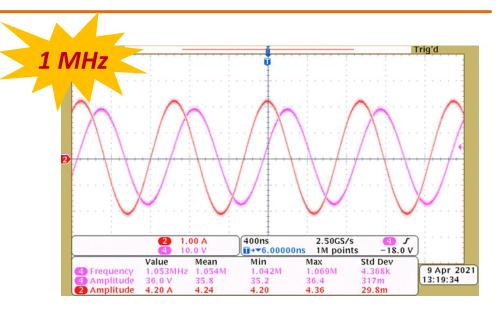
User Case #1: Multilevel Converters

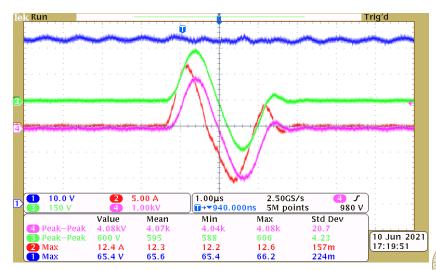
Pulsed Power Application





Continuous mode

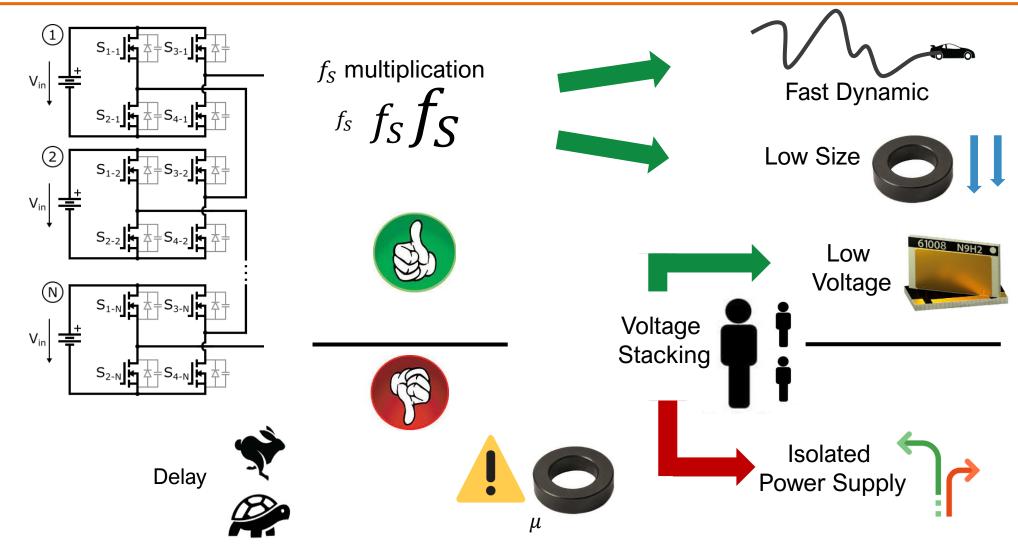






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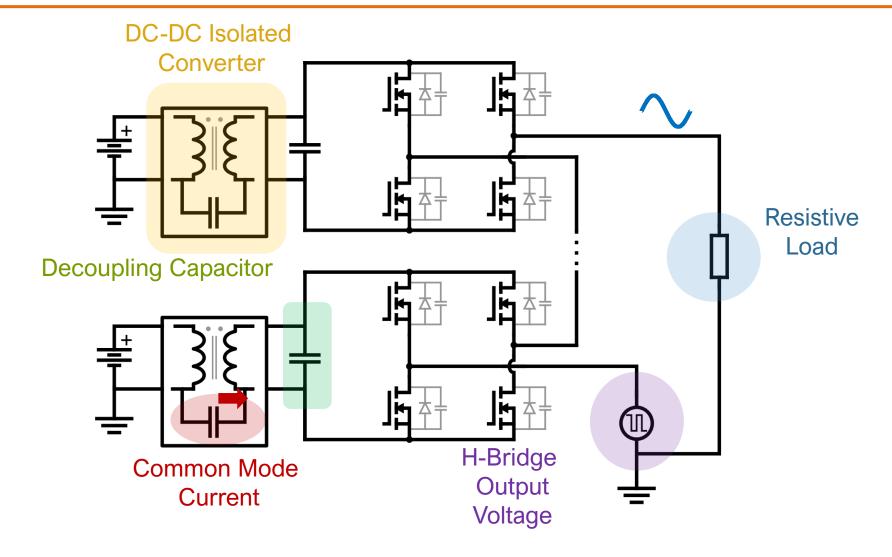
Proposed Topology: Cascaded H-Bridge







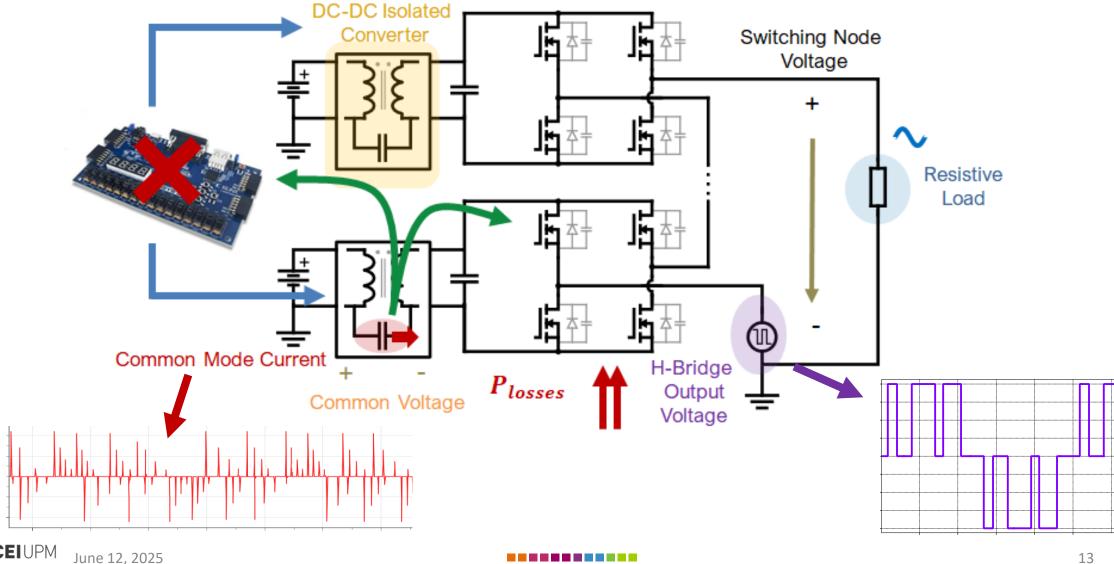
Challenges: Isolated Power Supplies







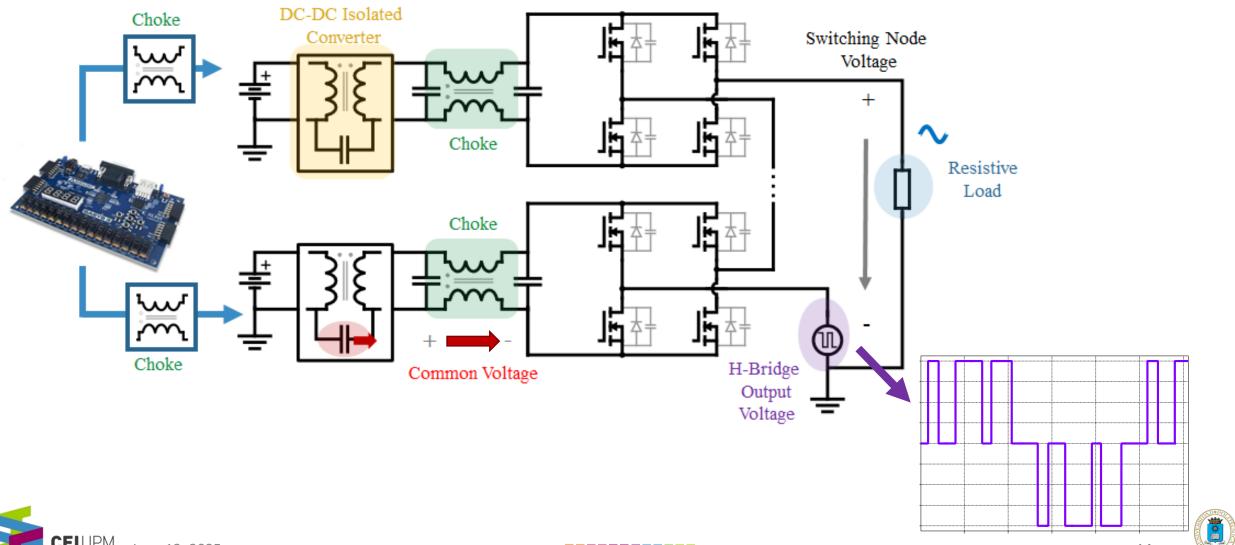
Challenges: Isolated Power Supplies





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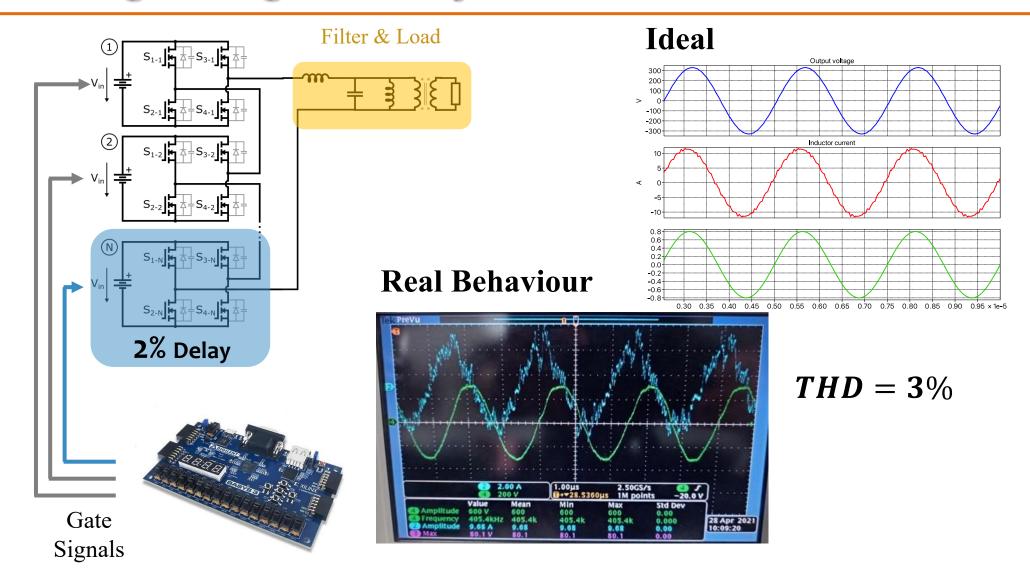
Challenges: Isolated Power Supplies



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GETUPM June 12, 2025

Challenges: Signal Delay

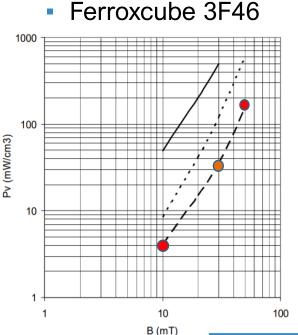




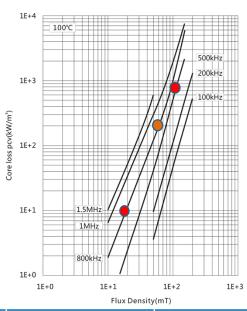


Challenges: Magnetic core - Material

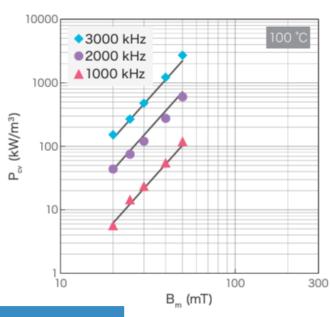
- Several possibilities for 1 MHz 2 MHz designs
- Due to high power loss density, the operating point will be far away from the saturation!







Proterial ML91S



 $B_{\text{max}} = 10 \text{mT}$ B_{may}=50mT **Material** $B_{max} = 30 mT$ ≈200 mW/cm³ Ferroxcube 3F46 4 mW/cm³ 40 mW/cm³ ≈7 mW/cm³ 90 mW/cm³ 300 mW/cm³ TDG TP5E 100 mW/cm³ 20 mW/cm³ Proterial ML91S ≈1 mW/cm³

In our experience we can dissipate up to 500 mW/cm³





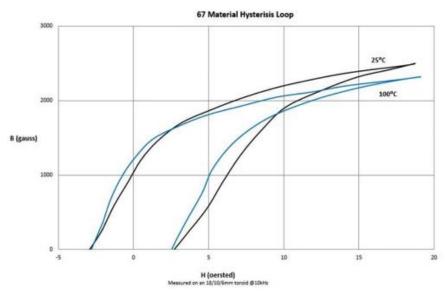
Challenge: Magnetic core - Material

NiZn Ferrite

Material 67
High Frequency Material

$$\mu_r = 40$$

$$f_{max} = 65 MHz$$



10 Gauss = 1 mT 1 Oe ≅ 80 A/m



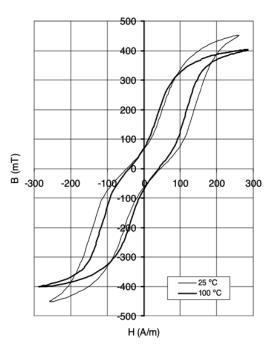
MnZn Ferrite

3F46

Medium Frequency Material

$$\mu_r = 750$$

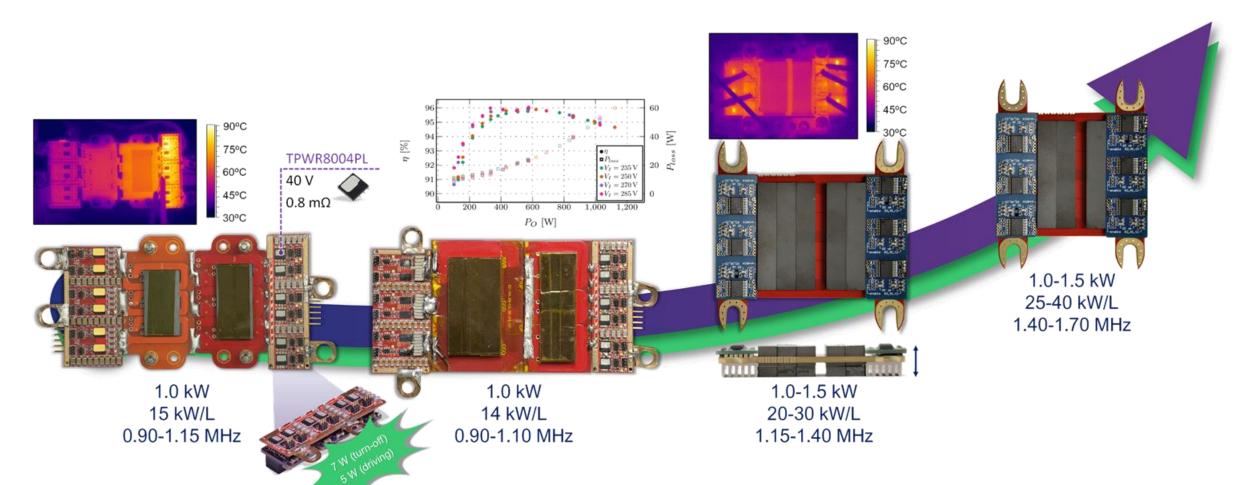
$$f_{max} = 3 MHz$$







It takes time, a lot of time!



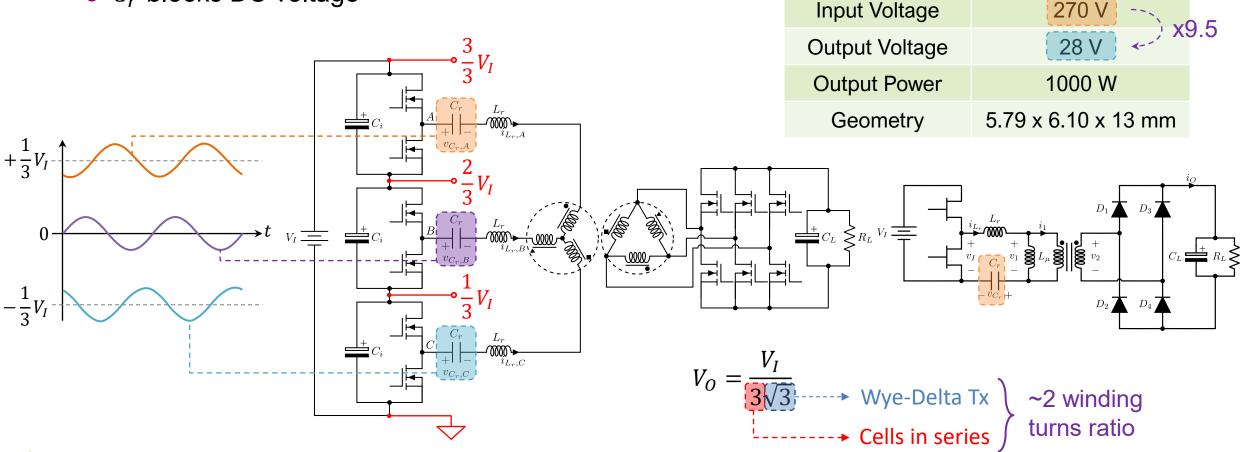


User Case #2: Wye-Delta Three-Phase LLC in Stack

Specification

A topology for high voltage step-down

 \circ C_r blocks DC voltage



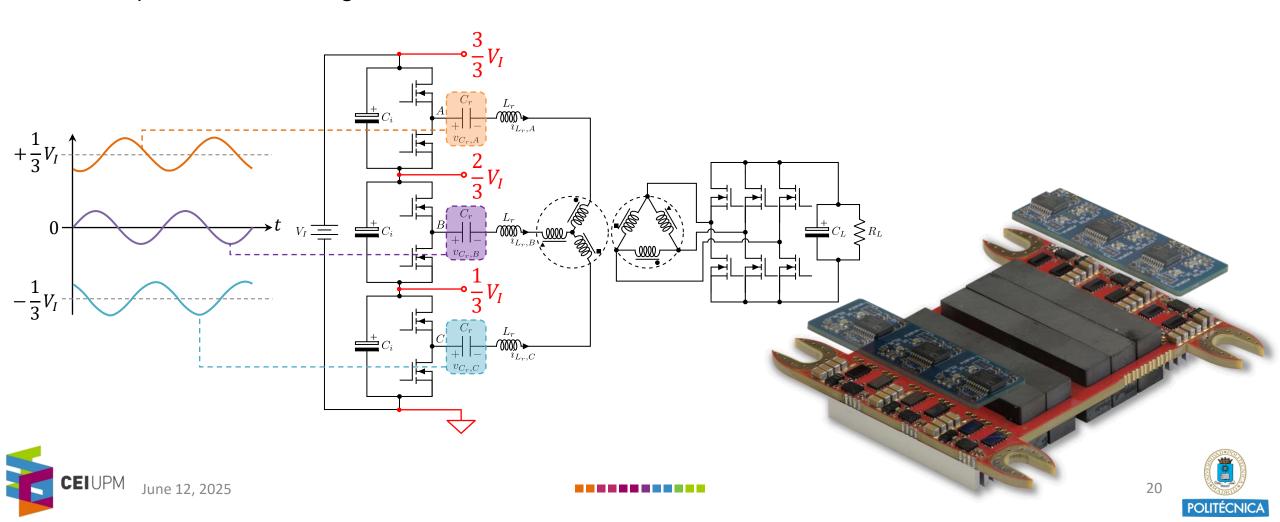




Nominal

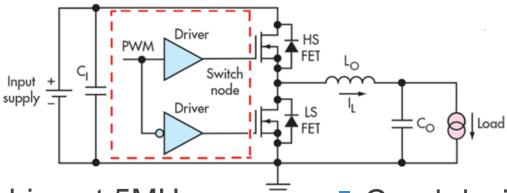
User Case #2: Wye-Delta Three-Phase LLC in Stack

- A topology for high voltage step-down
 - \circ C_r blocks DC voltage

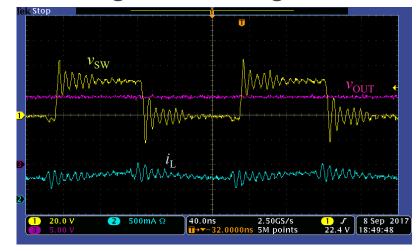


Challenge: Small Switching Loops

Switching loops must be very tight!

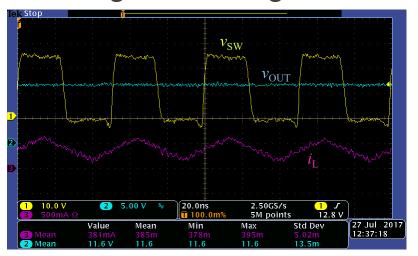


Bad design switching at 5MHz



Efficiency: 75.1%

Good design switching at 20MHz

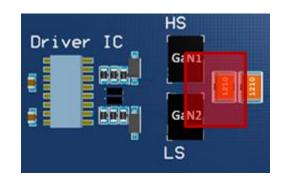


Efficiency: 83%

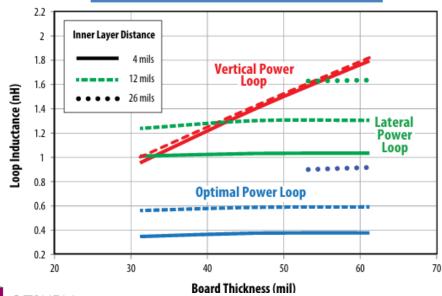


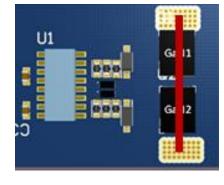


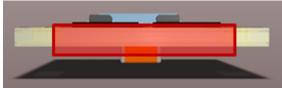
Challenge: Small Switching Loops



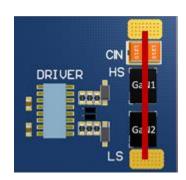
Lateral Power loop

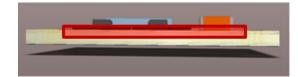






Vertical Power loop





Optimal Power loop

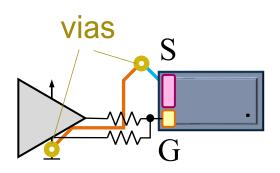




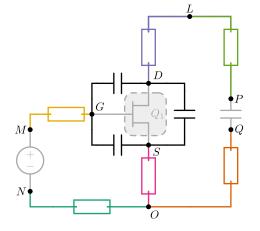
Challenge: Small Switching Loops

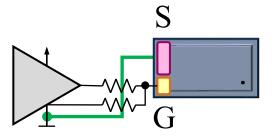
Meeting Efficiency and Power Density Goals - Driving technique

- Classical driving loop
 - The adjacent PCB layer is cut
 - Each via can add 1-2 nH of inductance
 - Flexibility in driver and on/off resistors
- 1-layer meander driving loop
 - Less usage of multi-layer PCBs (single layer)
 - No vias usage
 - Less inductance (faster switching)
 - Stiff driver and on/off resistors:
 - Driver with an accessible ground from 1 layer
 - > Jumping resistors (0603 on/off resistors)

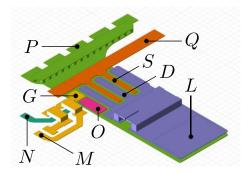


Classical: 3.7 nH





1-layer meander: 2.7 nH

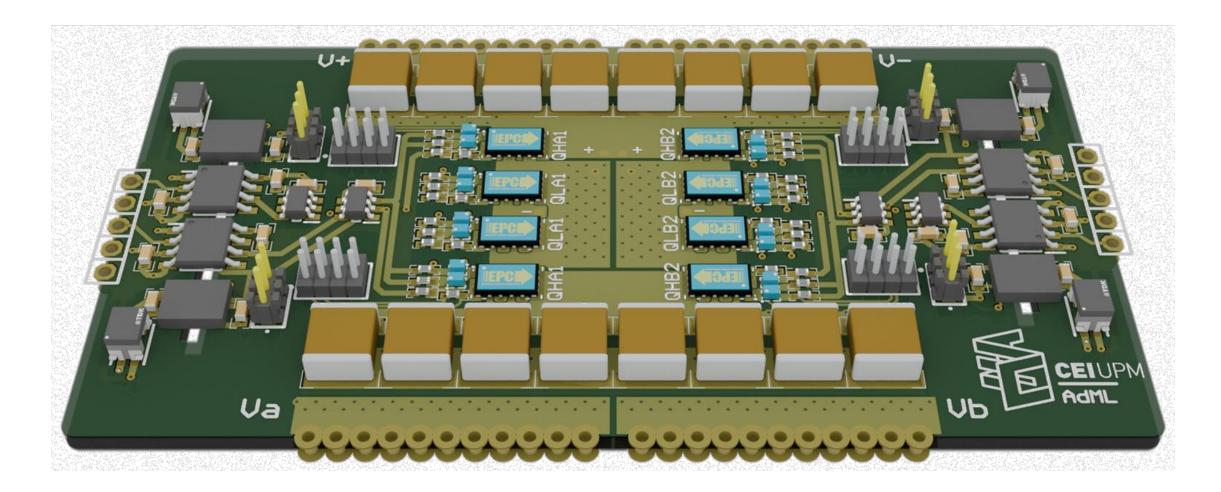


HFSS simulation





Challenge: How to place HEMTs in parallel?

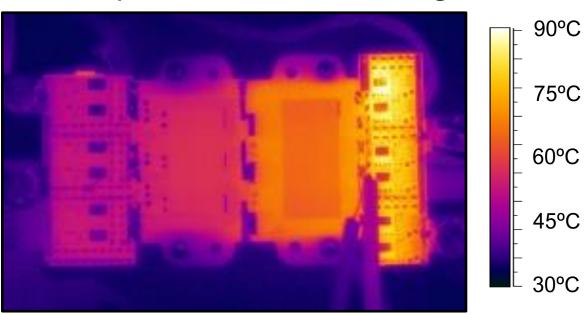




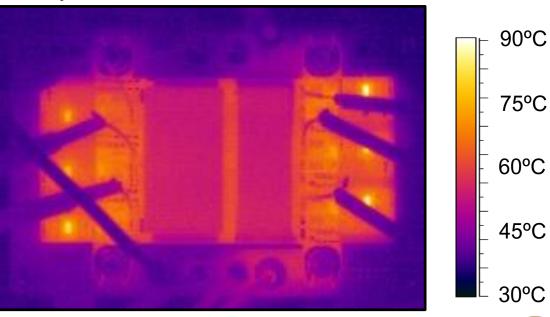


Challenge: Thermal Design

- Secondary side synchronous rectification
 - Low voltage → high current
 - Very high frequency (above 1 MHz)
 - Thermal coupling with the transformer windings (more copper)
- Not Optimised Thermal Design



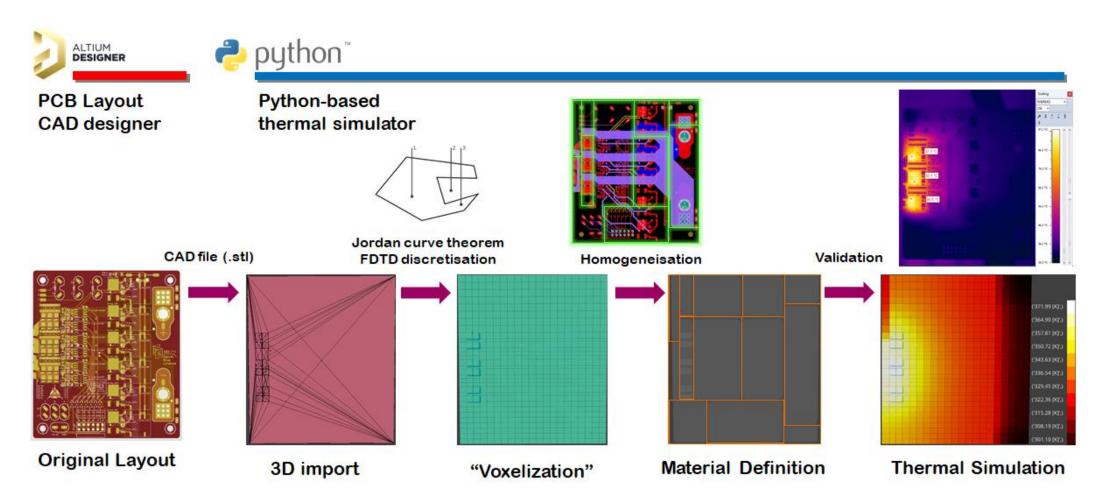
Optimised Thermal Solution







Possible Approach: Voxel-based Digital Twinning

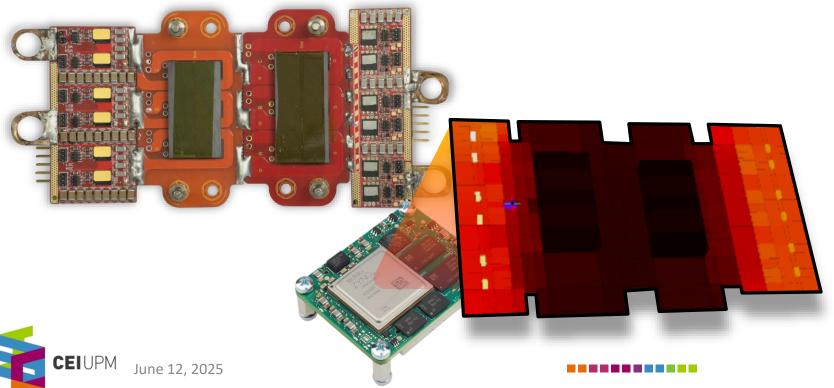


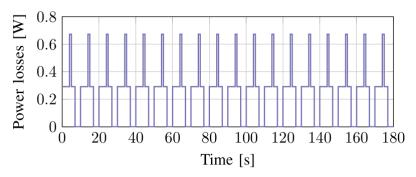


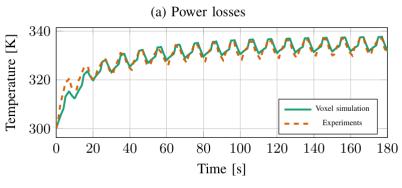


Possible Approach: Voxel-based Digital Twinning

- Digital replica of the real world power converter/system
- Real-Time Simulation-grade!
- Needs powerful computation hardware
- Al solver?





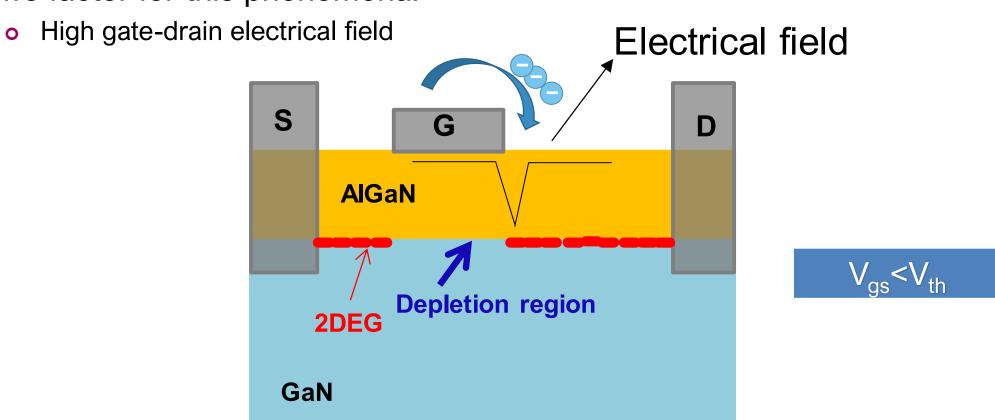


(b) Temperature trend of experimental results and voxel simulation





- Decrease of the 2D electron gas in the transistor channel
- Two factor for this phenomena:

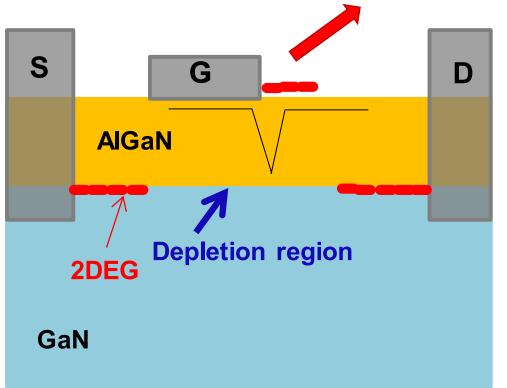






- Decrease of the 2D electron gas in the transistor channel
- Two factor for this phenomena:



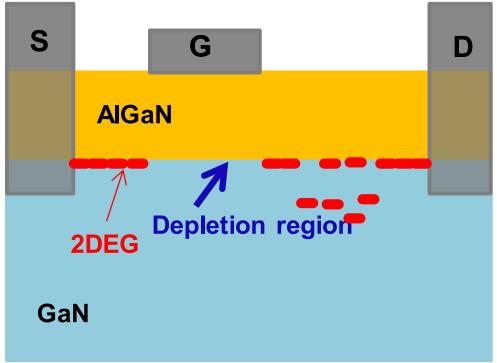








- Decrease of the 2D electron gas in the transistor channel
- Two factor for this phenomena:
 - High gate-drain electrical field
 - Deep trap electrons + hot electrons







- How to mitigate it?
- Decrease of the 2D electron gas in the transistor channel
- Two factor for this phenomena:
 - High gate-drain electrical field
 - Deep trap electrons + hot electrons

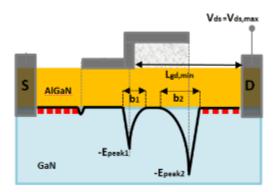
Depend on the blocking voltage

Passivation technology + field plate

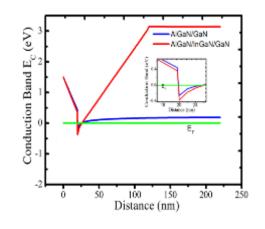
Buffer optimization (carbón doping, etc.)

At turn-on we need time to re-establish R_{ds DC}

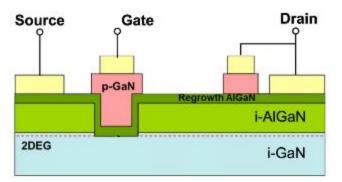
Field plate



Better confinement



Second p-doped drain contact

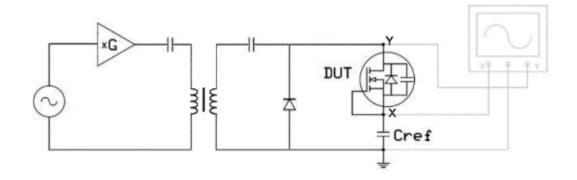




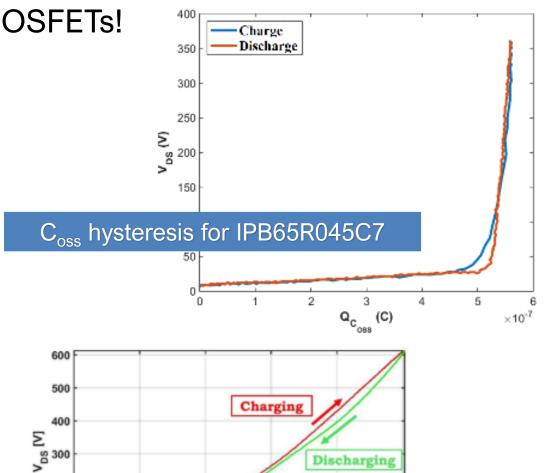


Challenge: C_{oss} Hysteresis

Well known phenomena in superjunction MOSFETs!



- Present with GaN Technology as well
- HEMT substrate plays a fundamental role
- Important impact at 10s of MHz!



C_{oss} hysteresis for PGA26E19BA



200

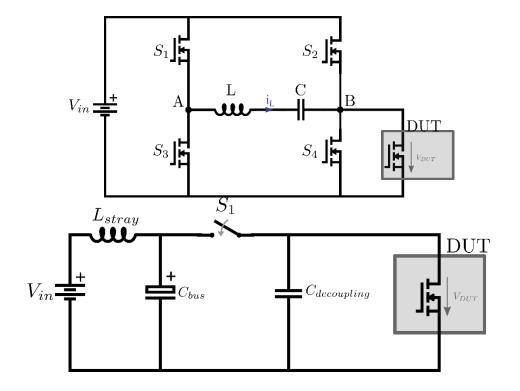
100

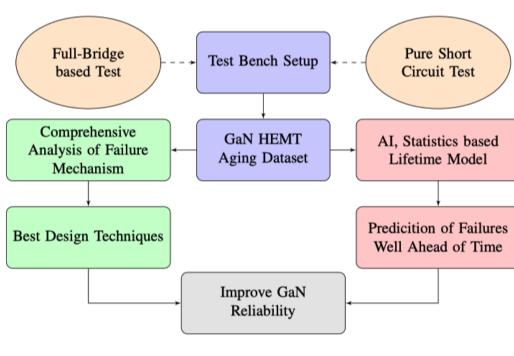
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Challenge: Short Circuit Capability

Following parameters are measured and analysed

- R_{DS_on}
- Threshold voltage
- dss
- gss



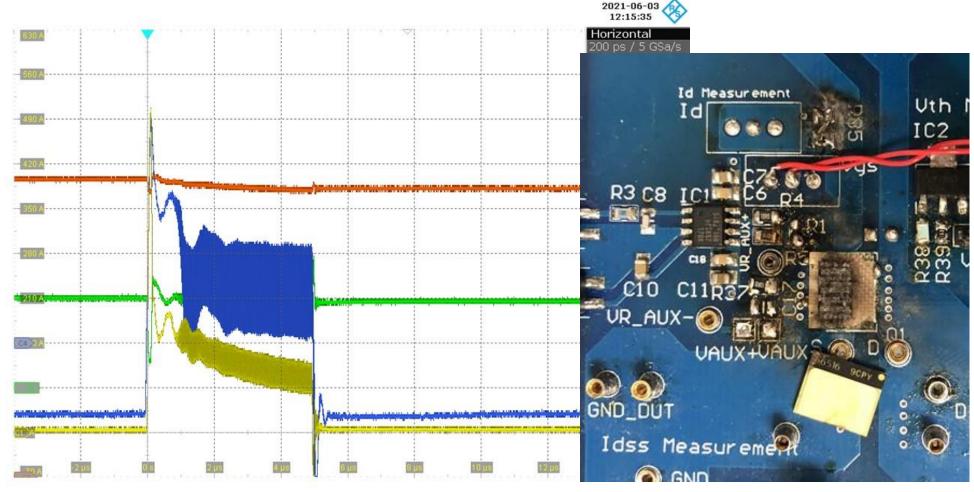






Challenge: Short Circuit Capability

Device becomes unstable after few short circuit events

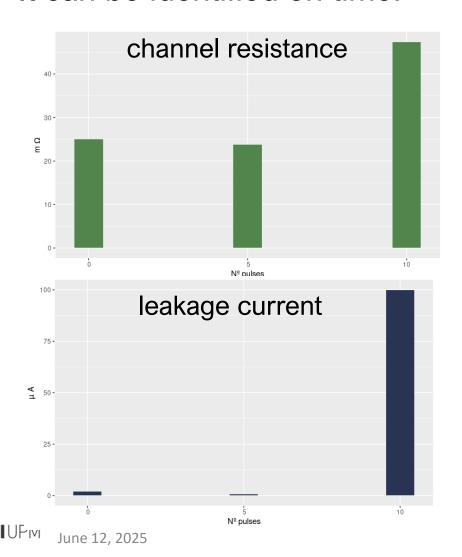


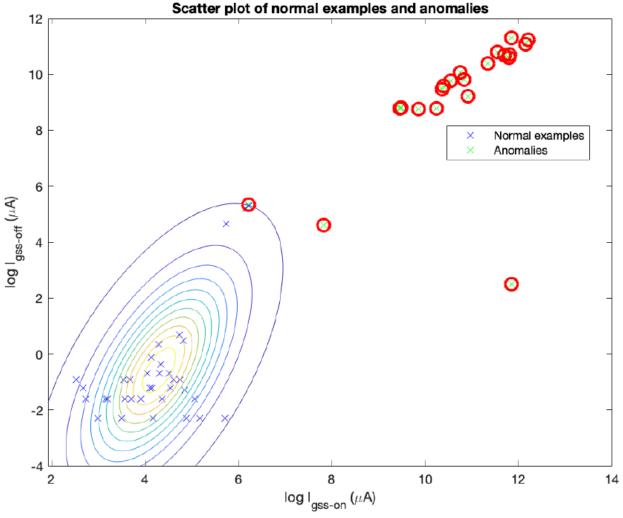




Challenge: Short Circuit Capability

It can be identified on time!









Research Opportunities and Directions

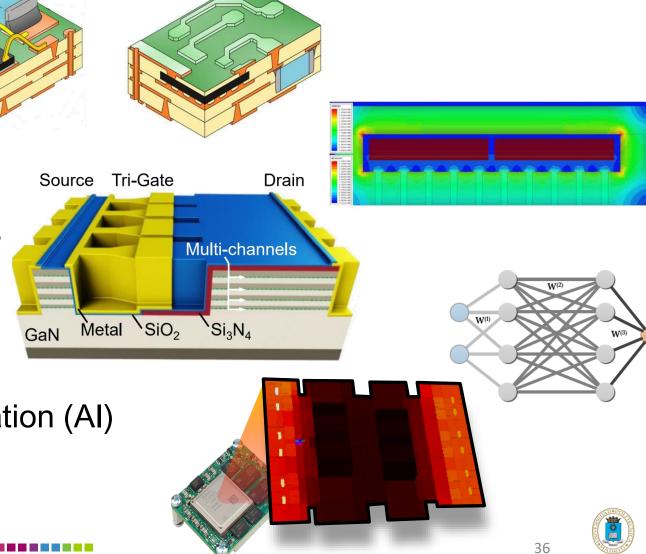
PCB embedded device

Advanced design of magnetics

Novel multigate/multichannel structures

Ultra fast protections

Digital Twin & Data driven health estimation (AI)





Thank you for your attention!





