BEYOND 200 Gbps: CHALLENGES AND PERSPECTIVES

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Data rate demands beyond 200 Gb/s PAM4 per lane are emerging from new applications such as Artificial Intelligence (AI) and machine learning (ML). Artificial intelligence high performance computing clusters have significantly impacted the physical infrastructure requirements of data center facilities. As the demand for data processing and storage continues to surge, these data centers are grappling with the challenge of evolving and expanding exponentially to keep pace with growth. The changing landscape of platforms, equipment design, architecture topologies, power density requirements, and cooling demands all underscore the pressing need for new architectural designs. Physical layer performance of the network data center must be improved by meeting many design challenges included but not limited to minimizing insertion loss and eliminating reflections while controlling the impedance environment throughout all copper interconnects. Moving to 400 Gb/s per lane requires a progression of materials, interconnects, and manufacturing methods as well as new system topologies. This work will explore these challenges and propose practical engineering solutions to fulfill the predicted 400 Gb/s per lane goals necessary for AI/ML large language learning models.

This work will explore various physical layer design improvements through simulation and modeling tools. Various design improvements will be explored including new copper cable assemblies, better SERDES signal processing, and better control of the characteristic impedance of the channel. Design case studies will be discussed that maintain an acceptable insertion loss in the 100 GHz range. This work will also review interconnect transition design to enhance channel performance. These critical tradeoffs shall be discussed herein to attain the higher bit rates demanded by new technologies.

The pros and cons for links operating at 400 Gb/s per lane will be analyzed, including the topics of potential obsolescence of components and media to enable the transmission of data with an acceptable Bit Error Ratio (BER). Front-panel connectors such as QSFP and OSFP, in their different versions, may no longer have adequate performance because of their inherent wipe tail created at the point of contact between the connector spring and the PCB microstrip finger. This wipe can create resonances as low as 60 GHz, well below the Nyquist frequency of 106.25 GHz in the case of PAM4 encoding. Several times in the past, copper cable solutions at increased bit rates were projected to be unfeasible, however, cable manufacturers were able to deliver acceptable solutions with a compromise of physical reach. This work discusses potential candidates to replace these traditional connectors, perhaps being replaced by embedded electrical-to-optical converters using co-packaged assembly substrates.

A way to achieve 424 Gb/s reliable operation could be by increasing the encoding level from PAM4 to PAM5, PAM6, PAM8, or even PAM16. Table I depicts the potential channel frequency baud rates and estimates for required slicer SNR and SNR components for different encoding levels relative to PAM4. Although on paper, increasing the encoding level would be

a reasonable path to increase the link rate, the required SNR increases as well as the impact of transmitter noise increase. A potential headwind is that since crosstalk is proportional to the derivative of the signal a component of noise from crosstalk is statistically reduced. The bandwidth ranges required for simulation and measurement are tied to the expected reference filtering. In the past the filtering cutoff frequency has been between the baud rate the Nyquist range. Work is needed to determine limitations caused by SNR and measurement/simulation bandwidth.

Table I.

Number of PAM levels	**4**	**5**	**6**	**7**	**8**	**16**
Baud rate (GBd)	225	200	180	163.64	150	112.5
Nyquist rate (GHz)	112.5	100	90	81.82	75	56.25
Estimate of increase of SNR required at slicer (dB)	0.0	2.0	3.6	5.0	6.1	12.1
SNR Increase in crosstalk contribution (dB)	0.0	0.7	1.5	2.5	3.5	5.2
Increase in snr impact for the transmitter noise component of noise at the slicer (dB)	0.0	3.9	7.6	11.2	14.7	28.0
Reduection in snr impact for the crosstalk component of noise a the slicer (dB)	0.0	4.6	9.0	13.1	17.0	31.3

Lack of physical scaling of traditional PCB based implementations to match SERDES capability and data rate demand suggests that front panel pluggable interfaces based on edge cards and baseboard routing may not be adequate to implement a 424 Gb/s bit rate link. New topologies and higher order modulation techniques have been presented as potential alternatives for exploration. Much work is still ahead to find adequate solutions both in hardware and software to enable communication channels operating beyond 212 Gb/s PAM4.

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[3] Y. Liu et al., "Inhomogeneous Dielectric Induced Skew Modeling of Twinax Cables," in *IEEE Transactions on Signal and Power Integrity*, vol. 2, pp. 94-102, 2023.

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[5] B. Gore, A. Josephson, R. Mellitz, F. de Paulis, L. Boluna, J. Calvin, R. Rabinovich, M. Resso, “Beyond 200G: Brick Walls of 400G links per Lane”, in *Proc. DesignCon 2025*, Santa Clara (CA), Jan. 28 – Feb. 30, 2025.