Emerging signal integrity issues in high-speed power electronics

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Summary

- Signal integrity: basic concepts
- Impact of the frequency on SI performance
- New trends in the power electronics technology
- A case-study: crosstalk noise in a power electronics board
- Co-simulation modelling approach
- Results and discussion

Acknowledgements

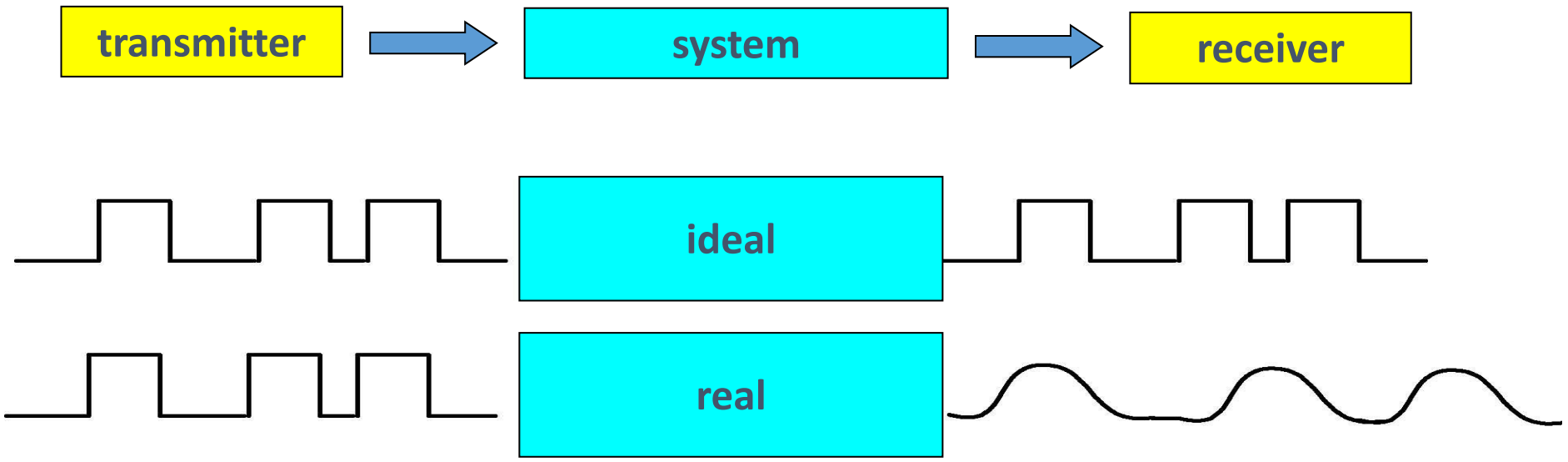
- Texas Instruments
- Keysight Technologies (Francesco Palomba, Hanqing Wen)

What is Signal Integrity?

SI is a measure of the changes experienced by an electrical signal passing through a system.

Changes may affect the **shape** and the **timing** of the signal.

If the waveform of the signal varies significantly from the original one, the receiver will not be able to read the signal.



Four main issues affecting SI in signal electronics

Impedance mismatch

An impedance mismatch along the signal path causes signal reflections. Besides adding noise to the signal, impedance mismatch can cause uncertainty in timing (jitter).

Crosstalk

Electromagnetic interaction due to conduction and induction phenomena, leading to unwanted coupling among different traces.

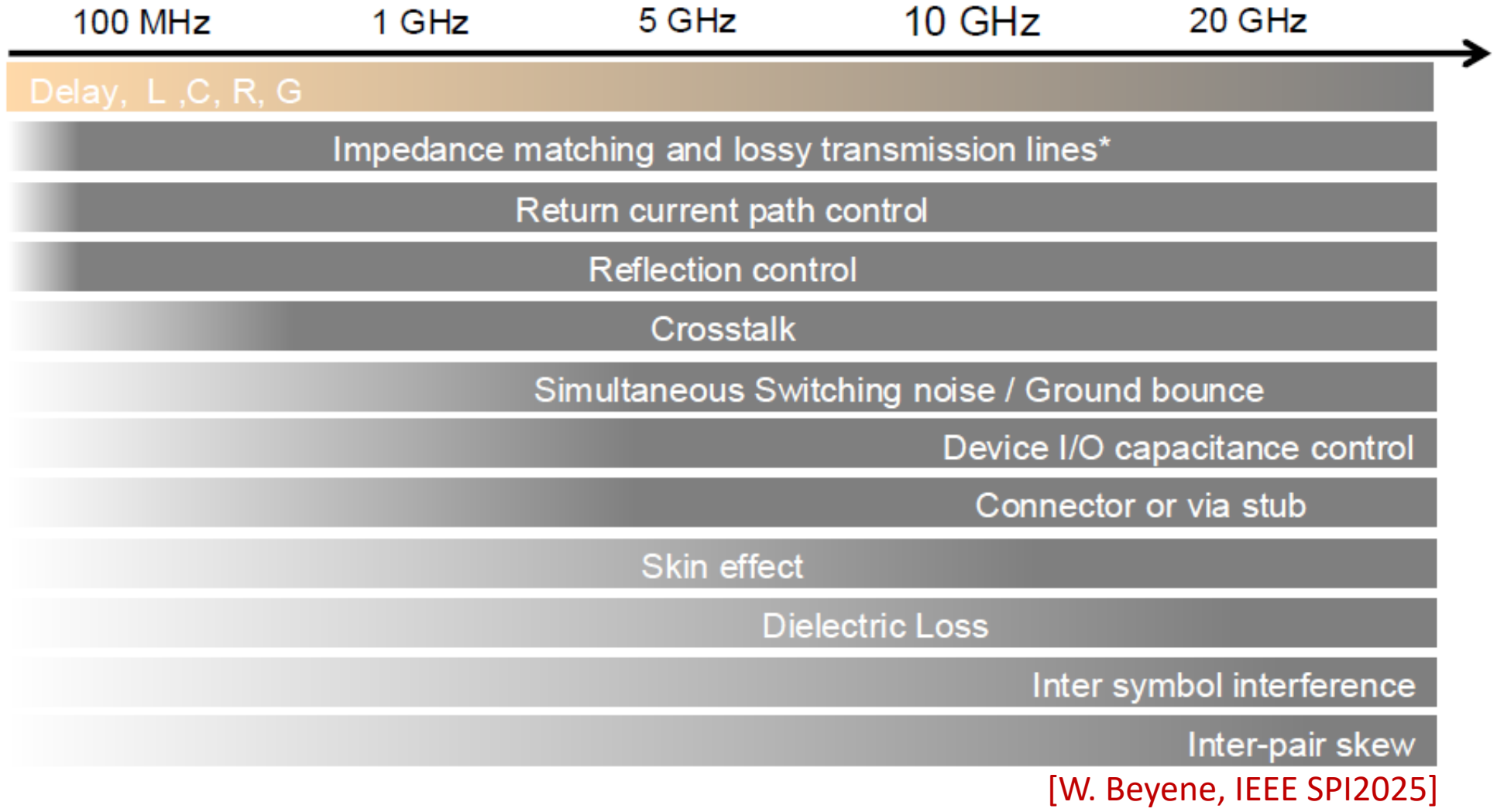
Electromagnetic interference (EMI)

Electromagnetic interaction due to unwanted radiation from circuit components (e.g., traces or vias), coupling to other circuit components in the same or nearby devices (interference).

Ground bounce

Ground potential fluctuations resulting in a drift of the reference for the low state. May be caused by multiple circuits switching between the high or low state at the same time (SSN).

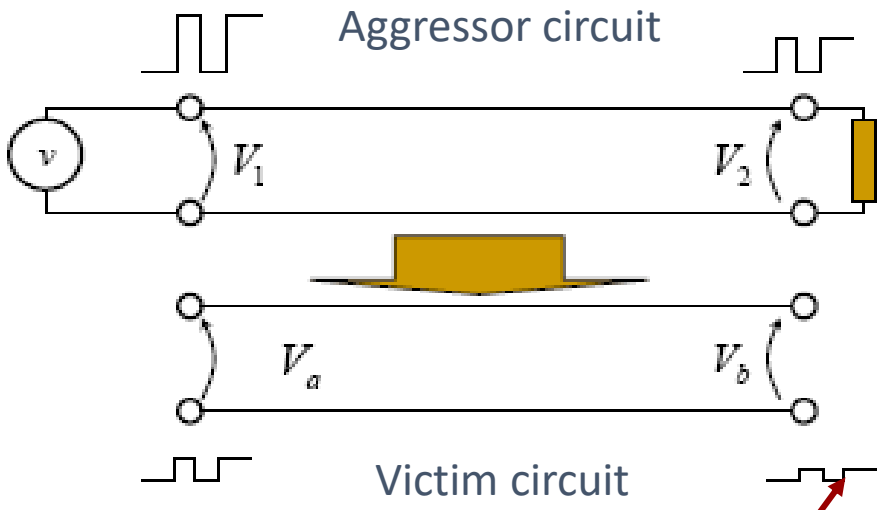
Signal integrity issues/challenges vs frequency



[W. Beyene, IEEE SPI2025]

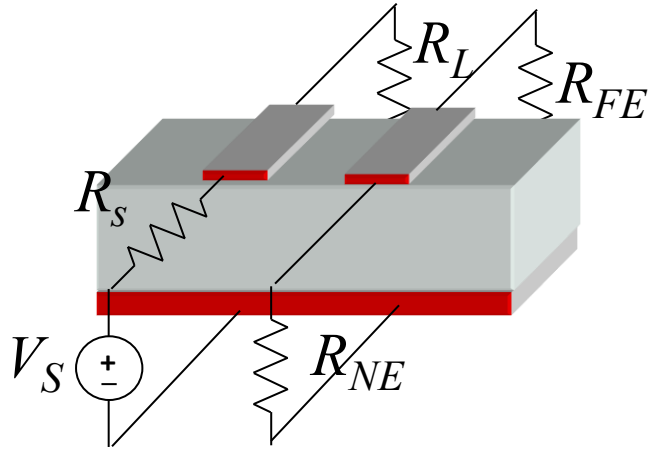
Higher frequencies and **smaller dimensions** exacerbate the SI issues

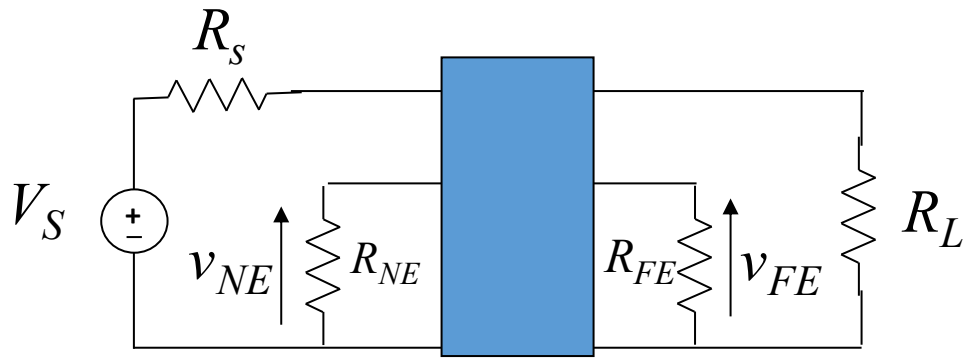
A simple crosstalk problem and the effect of frequency



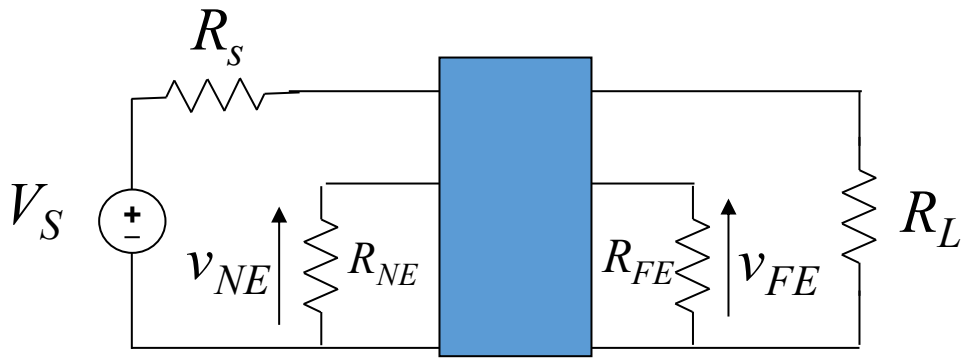
NEXT: near-end crosstalk

FEXT: far-end crosstalk

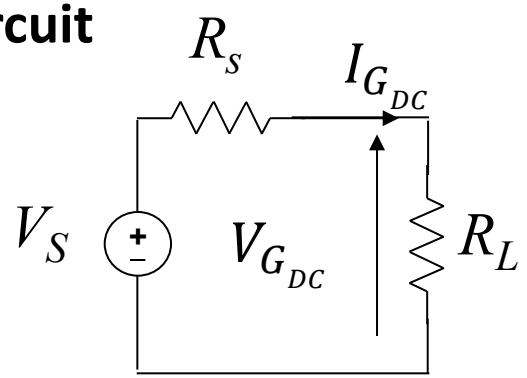




A simple crosstalk problem and the effect of frequency



Aggressor circuit



$$I_{G_{DC}} = \frac{V_S}{R_S + R_L}$$

$$V_{G_{DC}} = \frac{R_L V_S}{R_S + R_L}$$

Lumped model in the assumptions

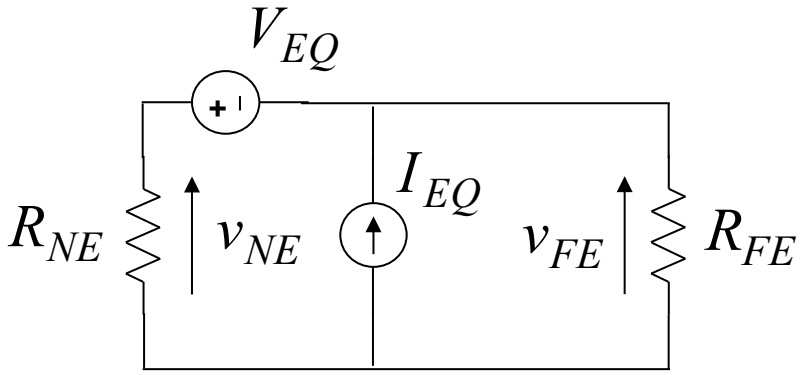
- ✓ Electrically short lines:

$$l << \lambda$$

- ✓ Weakly coupled lines:

$$\frac{L_m}{\sqrt{L_1 L_2}} << 1 \qquad \frac{C_m}{\sqrt{C_1 C_2}} << 1$$

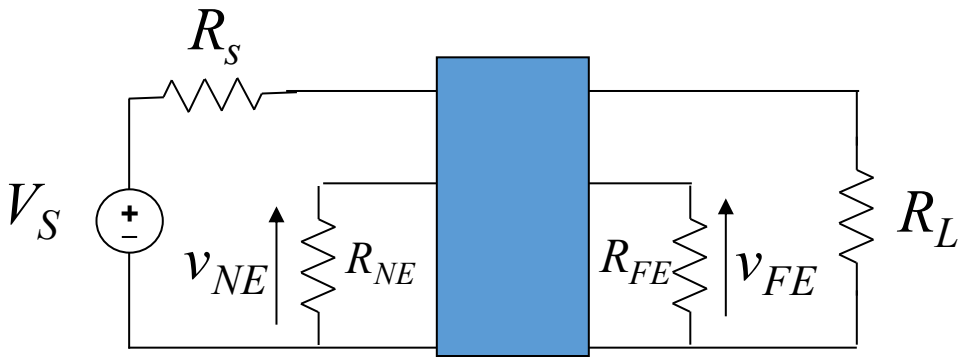
Victim circuit



$$V_{EQ} = j\omega L_m I_{G_{DC}}$$

$$I_{EQ} = j\omega C_m V_{G_{DC}}$$

Typical crosstalk problem: increasing frequency

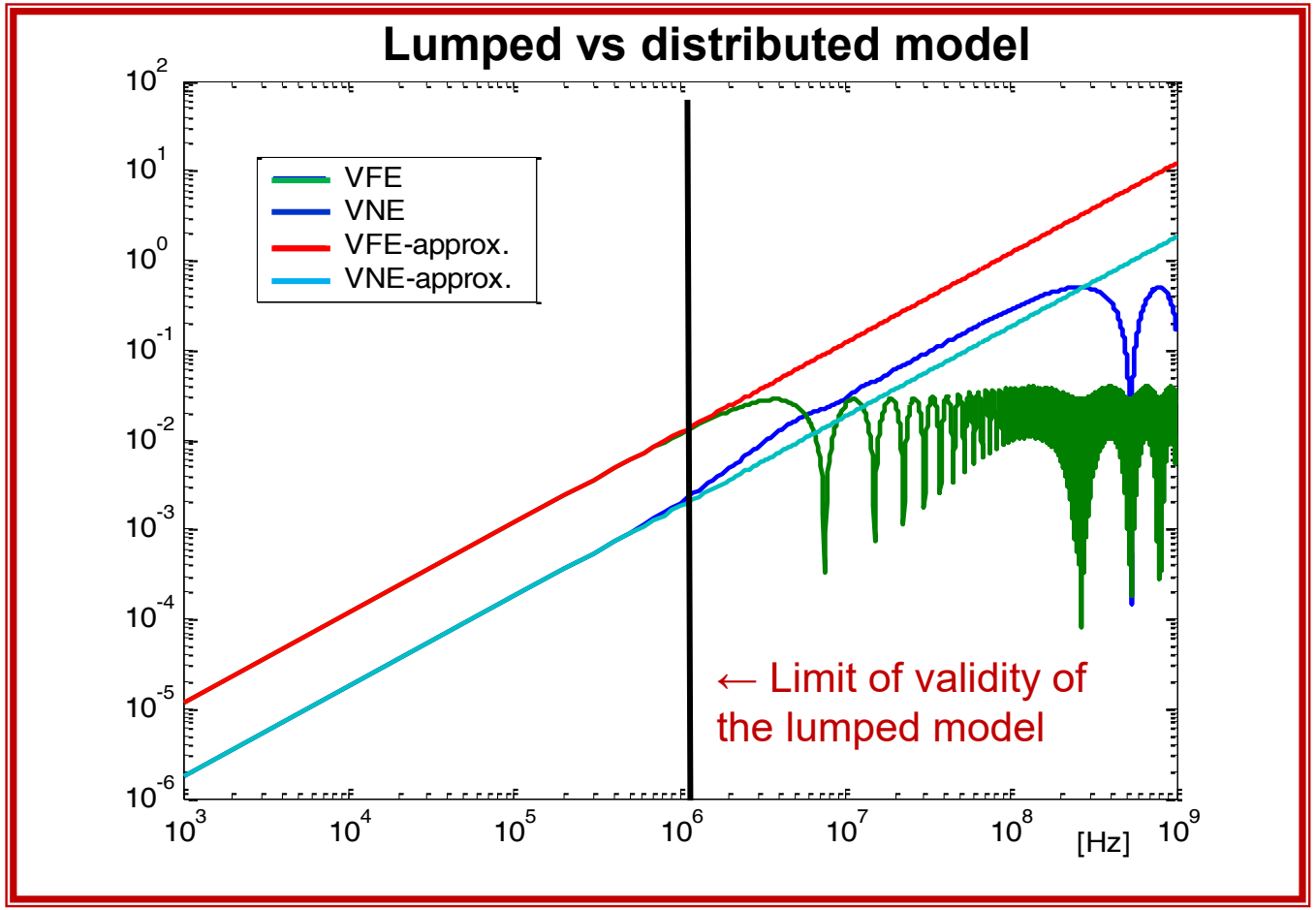


Lumped model

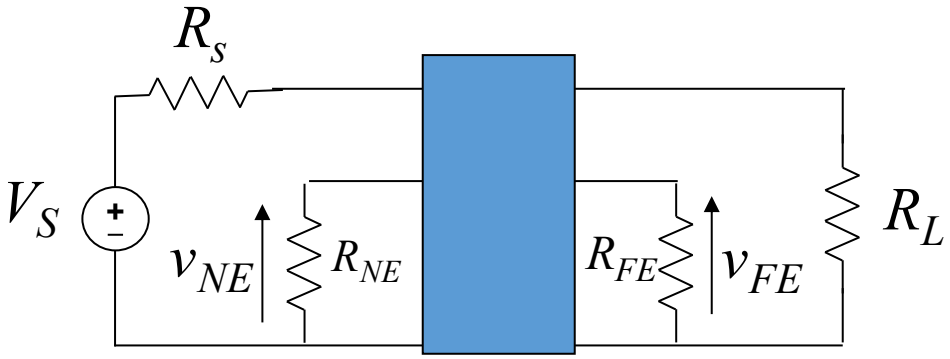
vs

Distributed model

(Transmission line model)



Typical crosstalk problem: effect of mismatching



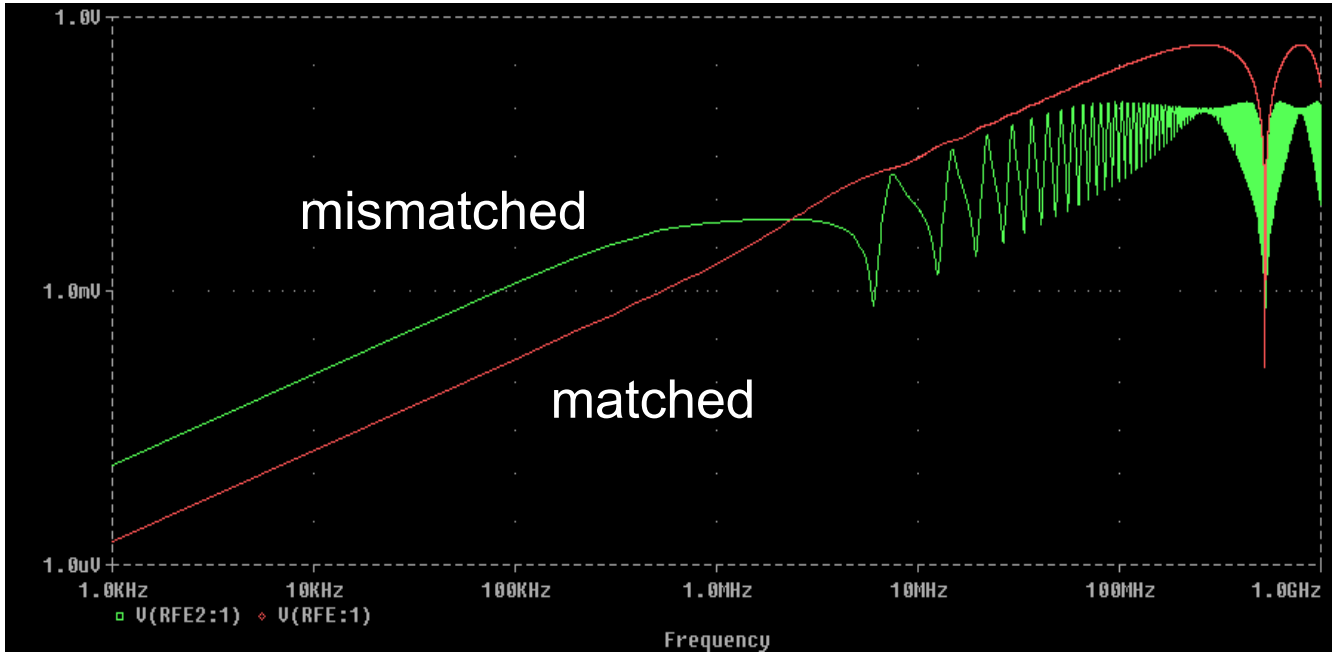
Matching condition:

$$R_S = R_L = R_{NE} = R_{FE} = Z_0$$

Z_0 line characteristic impedance

FEXT in matched vs mismatched case

$$R_{FE} = R_{NE} = R_L = 0.1Z_0$$

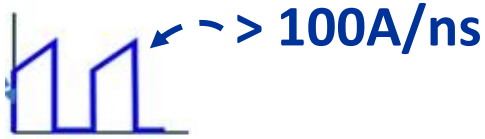


Crosstalk issues: signal electronics vs power electronics

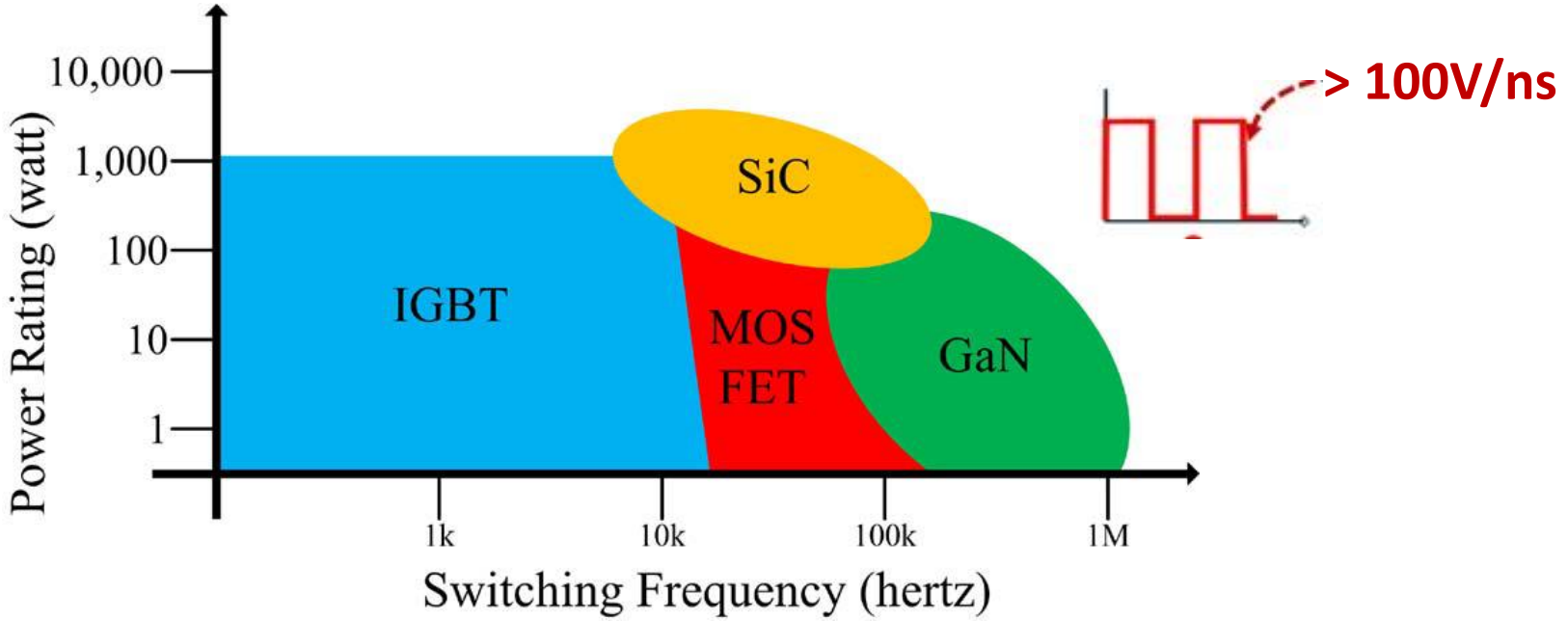
	Signal electronics	Power electronics
Frequencies	MHz–GHz	kHz–MHz
Impact	High (noise, distortion)	High (false switching, short-circuit losses, heating)
Main Causes	EM coupling among adjacent lines, mismatching, ground bounce	Fast switching, high slew rates, parasitics
Mitigation measures	Differential signalling, shieldings, optimized PCB layout (trace spacings, loop reductions,..)	Snubber, gate drivers with negative voltage shutdown, compact layout to reduce inductances

Is this still valid?

Trends in power electronics



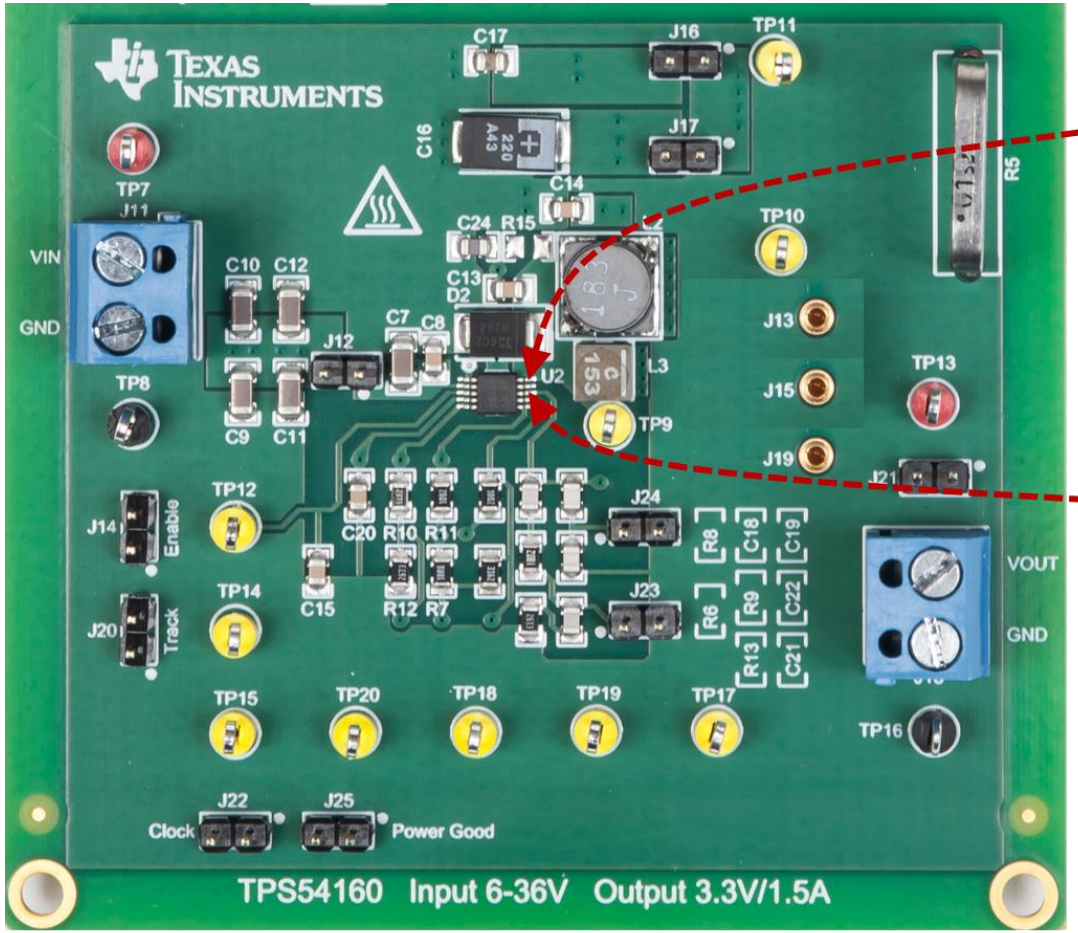
- New devices (GaN, SiC)
- Higher switching frequencies,
- Higher slew-rates
- Higher power density (power/volume)



No longer possible to analyze SI issues (such as crosstalk noise without taking into account the distributed nature of the circuits

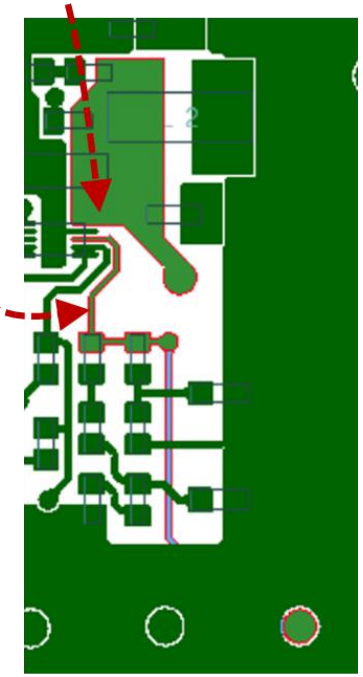
Power to control crosstalk in Switch-Mode Power Supplies

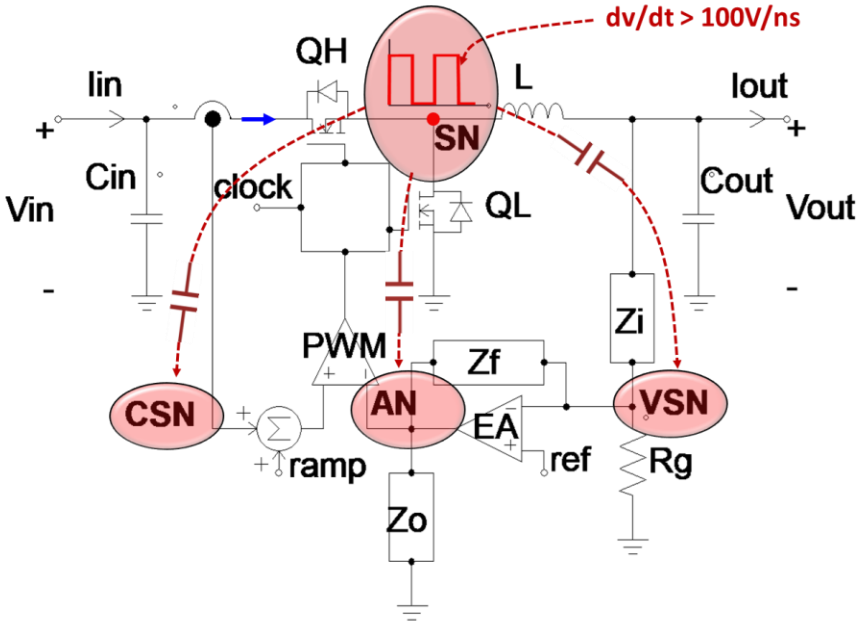
A case-study: TI-PMLK BUCK board



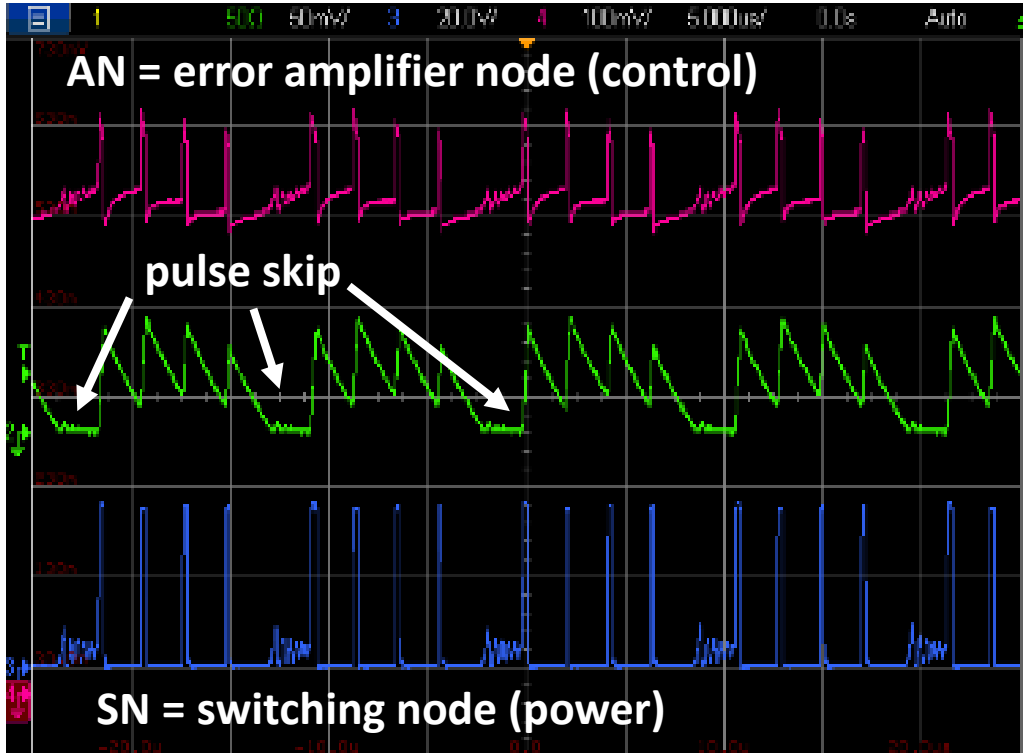
https://www.ti.com/tool/PMLKBUCKEVM

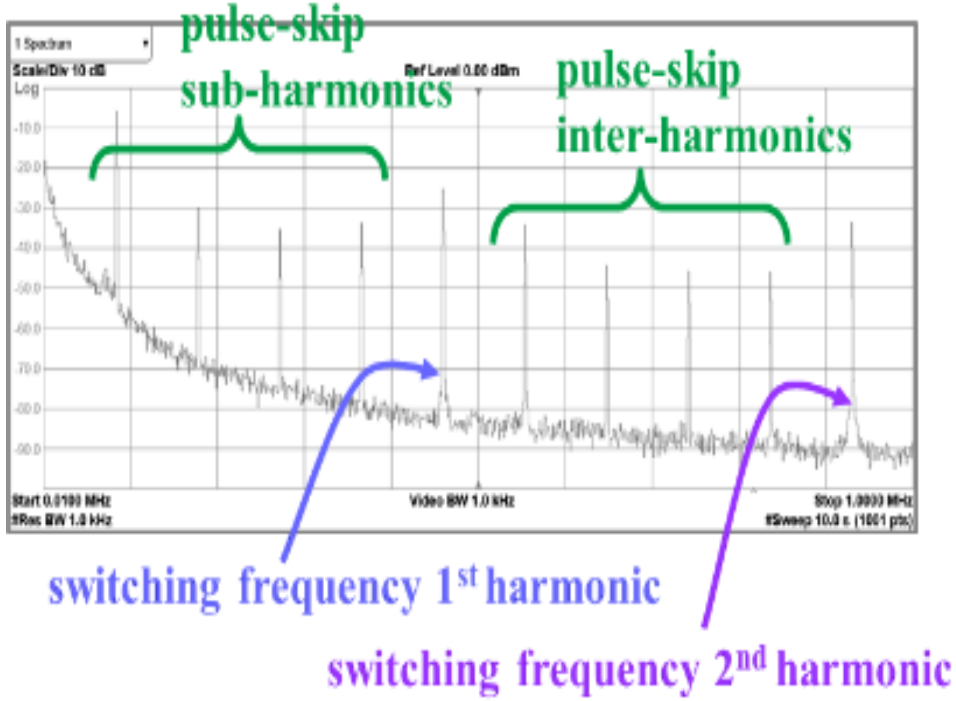
SN: switching node (power)
AN: amplifier node (control)





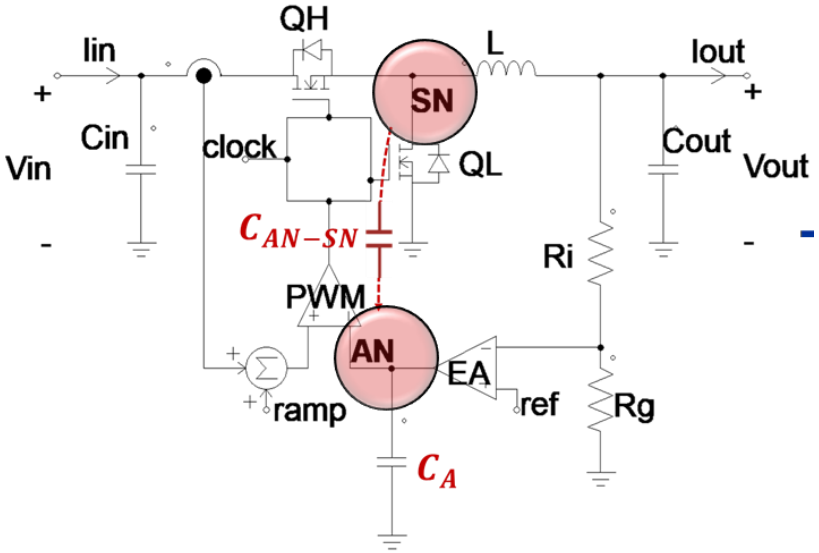
Power to control crosstalk in Switch-Mode Power Supplies

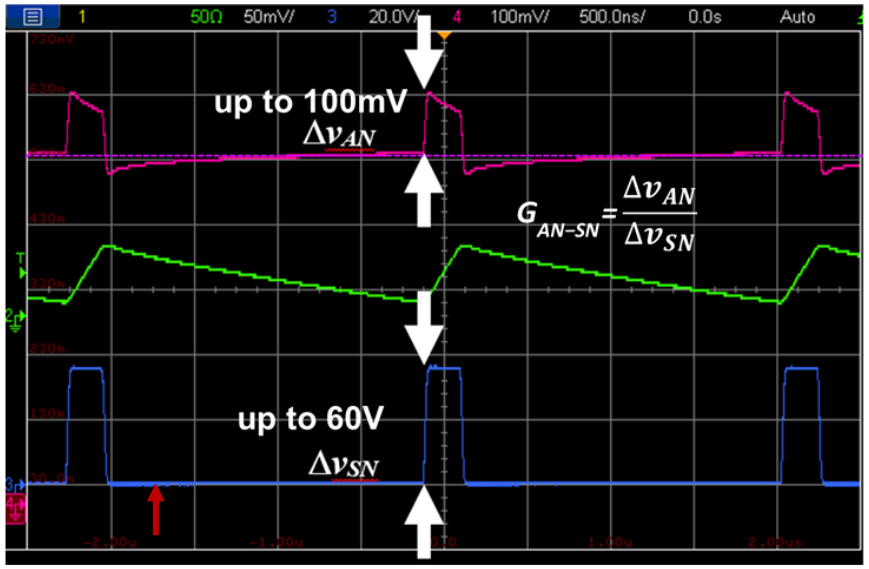




SN to AN coupling may result in problems in the control, with issues like pulse skip

A simple model: lumped coupling capacitances





derived from measurements

$$G_{AN-SN} = \frac{\Delta v_{AN}}{\Delta v_{SN}}$$

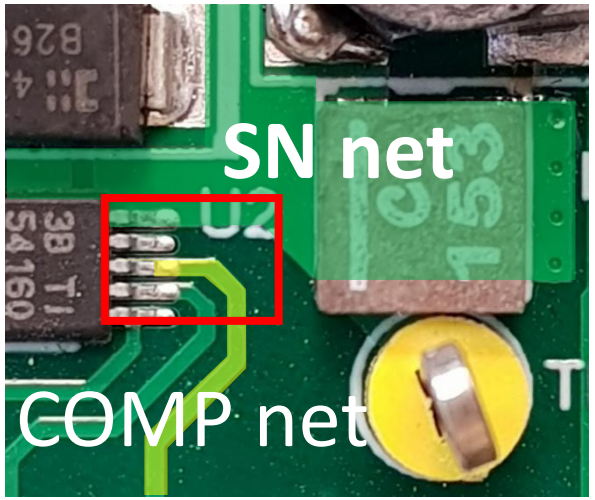
$$C_{AN-SN} \cong C_{AN} \frac{G_{AN-SN}}{1 - G_{AN-SN}} \cong 10 - 100 \text{ fT}$$

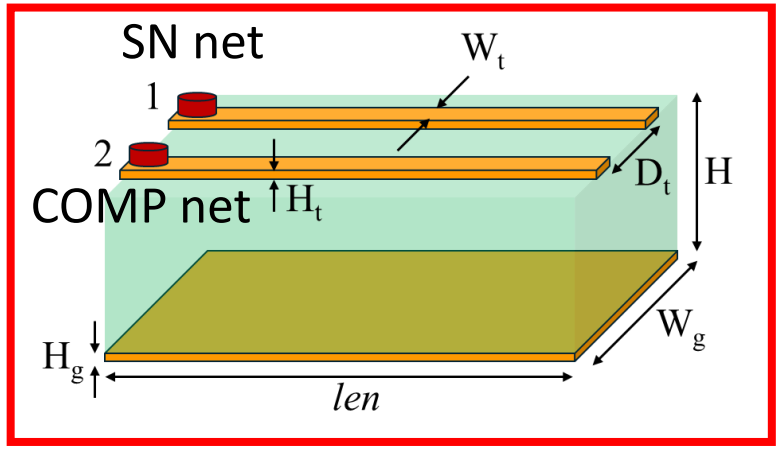
Limits:

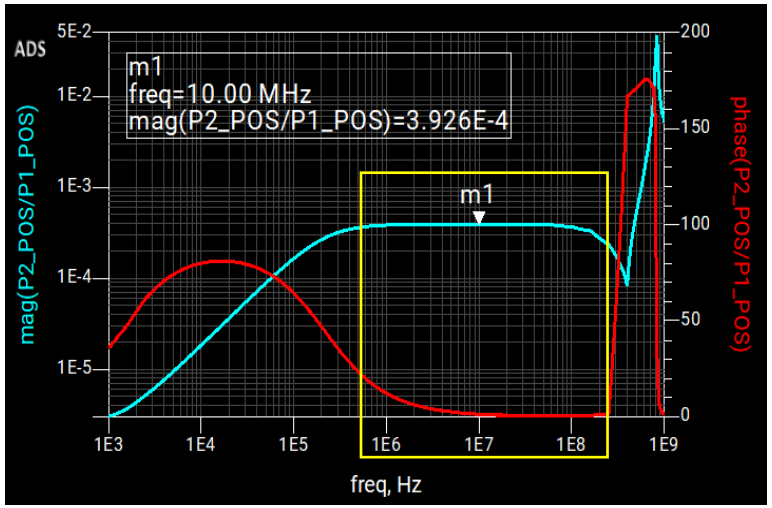
- It onlyprovides a coarse approximation
- Does not account for distributed effects
- Does not account for resistances and inductances

[G. Di Capua, APEC2022]

A higher-order model: distributed coupling capacitances







Simulation tool	Coupling capacitance (fF)
Comsol 2D	11.4
Comsol 3D	11.0
ADS CILD	12.2
ADS TL	12.3
PEPro Mom RF	12.3
PEPro MomMW	12.9

$$C_m = -\frac{imag(Y_{m21})}{2\pi f}$$

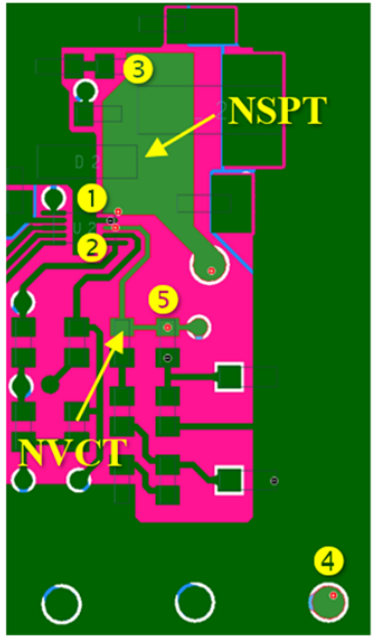
[G. Di Capua, SMACD2024]

Limits of the approach

- It is only valid in a limited frequency range
- Do not account for resistive and inductive effects

A distributed model approach: co-simulation

- The EM behavior (couplings) is captured by a full **3D numerical field solver** (e.g., MoM, FEM), providing the **S-parameters** referred to the chosen ports;
- The S-parameters are used to synthesize **an equivalent circuital multiport**, a “box” to be embedded into the overall circuit model
- The crosstalk analysis can be now carried **at system level** taking into account the devices actually connected to the ports.



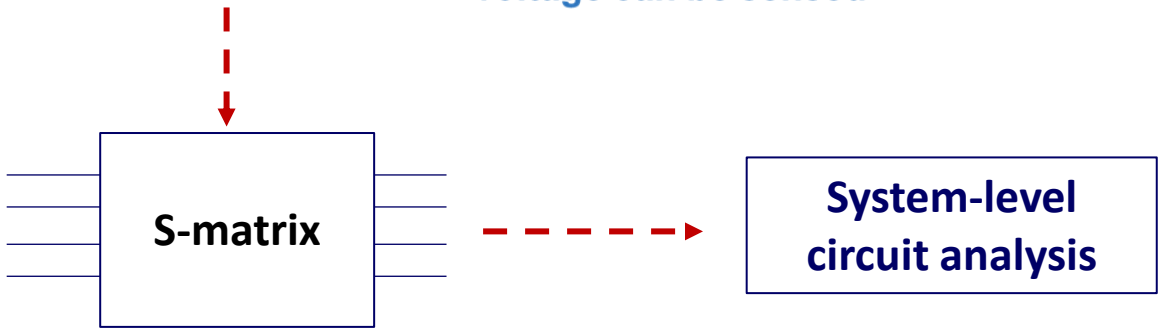
❶ = SN, where noise is injected
NSPT = Noise Source Power Trace,
PCB area disseminating the SN noise

❷ = AN, where noise is received
NVCT = Noise Victim Control Trace,
PCB area harvesting the SN noise

❸ test point where the SN voltage is sensed

❹ test point where the AN voltage can be sensed

❺ second test point where the AN voltage can be sensed



Modelling the PCB: not an easy task …..

CAD model: in principle, it must include:

- The nets of interest and any other potentially involved
- The power and ground routing layers
- The package layers and the silicon substrates
- The surrounding structures, bond/bump pads

EM solver:

- FEM, MoM, etc… (pro and cons)

Meshing:

- Proper meshing may require large numbers of elements
- Not trivial to define the regions where the mesh must be refined

Port definition:

- Defining the ports for the EM model is a crucial task
- Not trivial to identify the right place to place the reference pins for the ports

Circuit block synthesis:

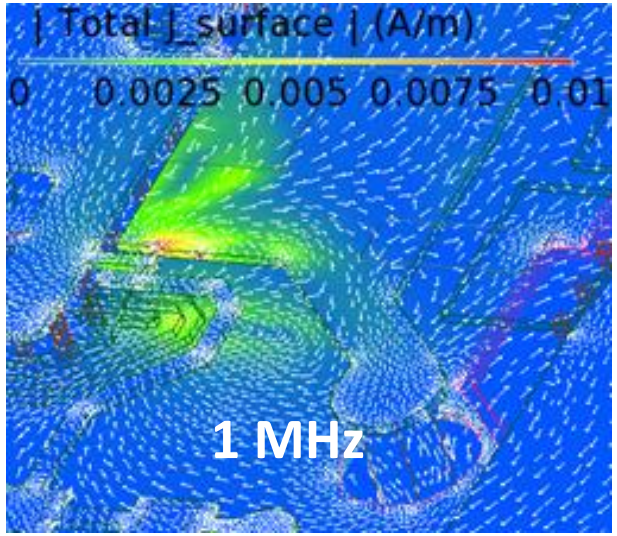
- Model order reduction
- Passivity enforcement
- Broadband validity

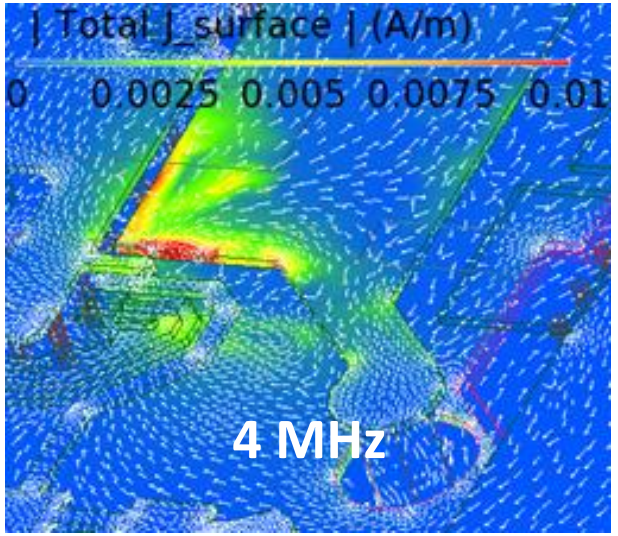
EM simulation: current paths vs frequency

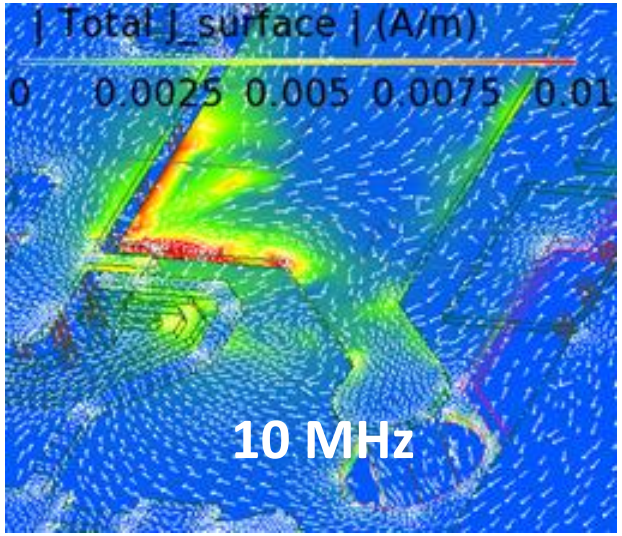
-as the frequency increases more layers are involved in the current return path

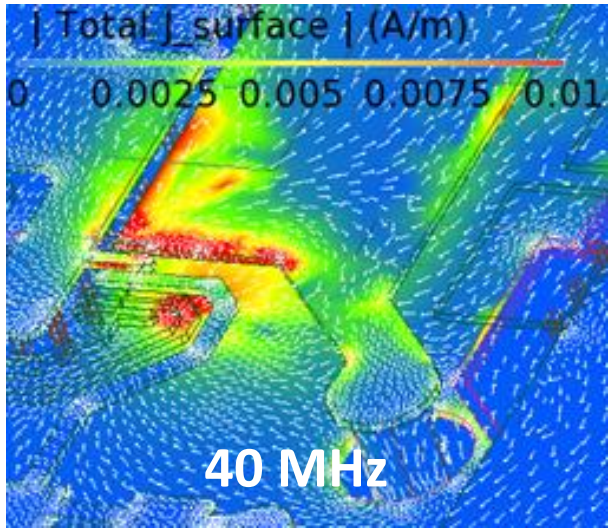
- large conductive areas (pads, grounds) are the main responsible for capacitice coupling

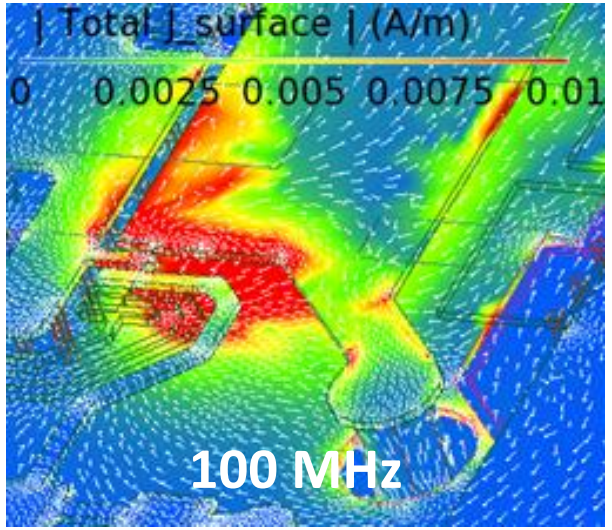
-inductive and conductive coupling takes place also through the vias

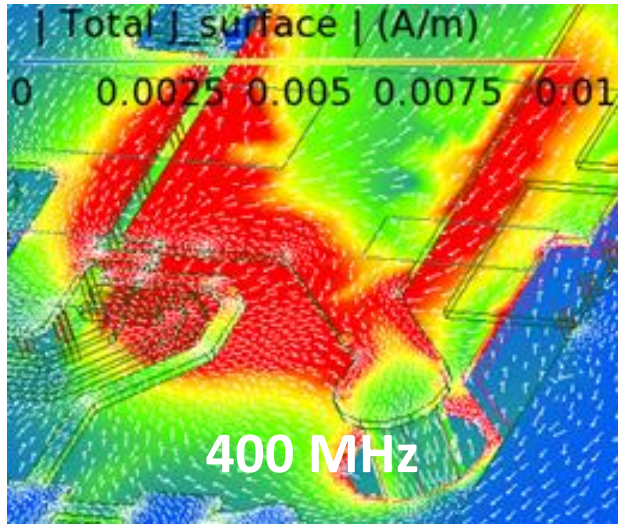




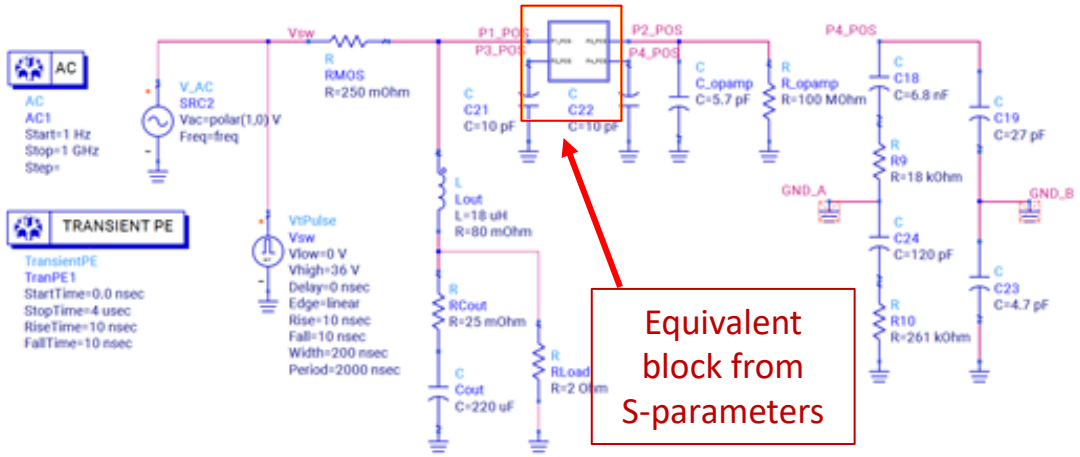








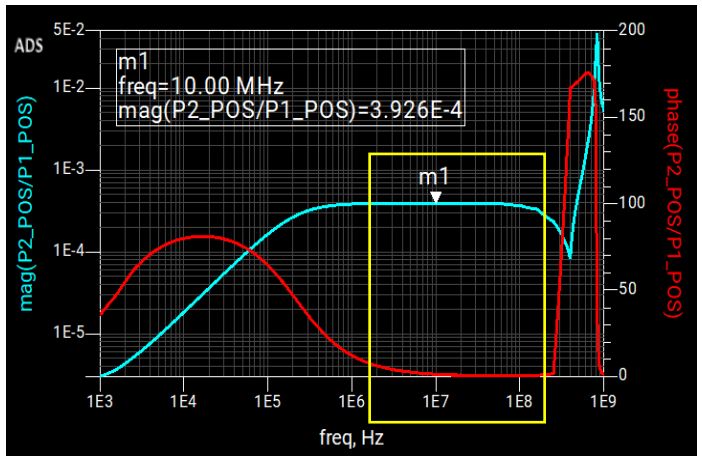
System-level analysis of the xtalk



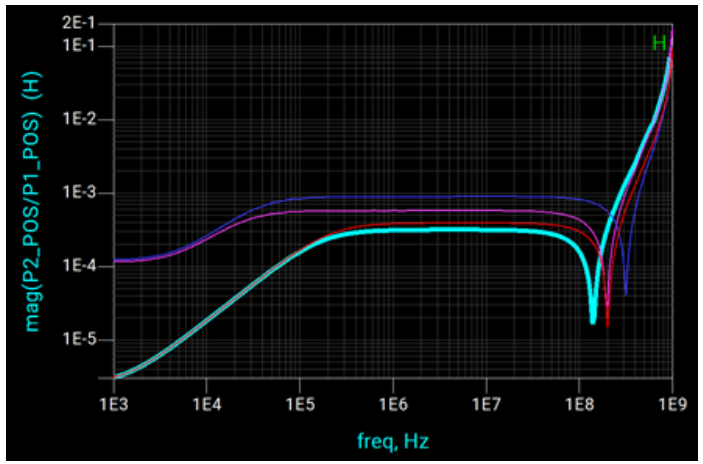
- The noise if capacitive only in a limited range of frequency
- Inductive and resistive effects are evident in the low and high frequency ranges
- Measuring the noise is challenging since the probe impedance may be comparable to the parasistics

noise gain vs frequency

$$G_{AN-SN}(f) = \frac{\Delta v_{AN}(f)}{\Delta v_{SN}(f)}$$



ports 3 & 4 open



ports 3 & 4 closed on the probes

Can we apply the standard design guidelines for SI inspired from the Signal Electronics?

	Signal electronics	Power electronics
Trace dimensions and separation, layer thickness	Design driven impedance matching, 3W-rule for spacing, etc..	Design driven by the thermal management and by dI/dt (slew-rate)
Pad areas	Reduce as much as possible to lower parasitices	Trade-off between thermal management (↑) and dV/dt (↓)
Ground planes	Increase the number to shield the more aggressive nets (e.g., clock)	Trade-off between thermal management (↑) and common mode noise (↓)
Ground cuts	Avoid cuts and discontinuities in the ground that interrupt the return paths	Two separate grounds electrically connected but equipotential (no current flow)

Which of the SE guidelines will be implemented in PE?
Would PE- SI require new solutions?

Conclusions

- **Power electronics** applications based on **GaN and SiC devices** are characterized by **higher frequencies**, **faster slew rates**, and **smaller, more compact dimensions**.
- While these technologies offer significant advantages, they also introduce **major challenges in terms of signal integrity (SI)**, similar to those encountered in signal electronics.
- The traditional approach of analyzing SI in PE by considering only the **parasitic effects of components** is no longer sufficient. At high frequencies, **distributed effects within the PCB play a crucial role**.
- **Co-simulation (EM + circuital**) has become a key method for analyzing these issues from the early design stages. However, applying this approach to real-world applications is not trivial.
- **Classical solutions** used to mitigate SI issues in signal electronics **may not be directly applicable to power electronics**, where the design has traditionally been driven by different objectives.
- **There is a need of original approaches to face these challenges!**


Thank You !